# SEQUOIA Device Designer ESD

## Predictive simulation of
## Electrostatic Discharge - ESD protection circuits

## Overview

Effective analysis and design of ESD protection circuits is an issue of significant and growing importance for VLSI design and manufacturing. Inadequate ESD protection can result in costly product failures in the field, while over-designed protection circuitry would waste valuable silicon area. In-depth understanding of the ESD event is essential to making fundamental decisions about the type and configuration of protection devices and circuits.

SEQUOIA Design Systems, Inc. provides fully integrated physical level simulation software for this crucial task. Simulation is carried out on mixed-mode device-circuit level. Multiple devices are analyzed at the level of partial differential equations (PDE) including all relevant effects such as impact ionization, self-heating, bipolar parasitics, snap back, etc. Connections between devices and additional circuitry are described by SPICE-like circuit-level models. The software system has a powerful graphical user interface, is easy to use, and allows to get meaningful results fast. Circuit schematics are drawn using the built-in schematic editor. Extensive simulation studies varying a number of physical parameters can be easily set up and executed, built-in optimization provides tools for a precise determination of circuit configurations for specified goals.
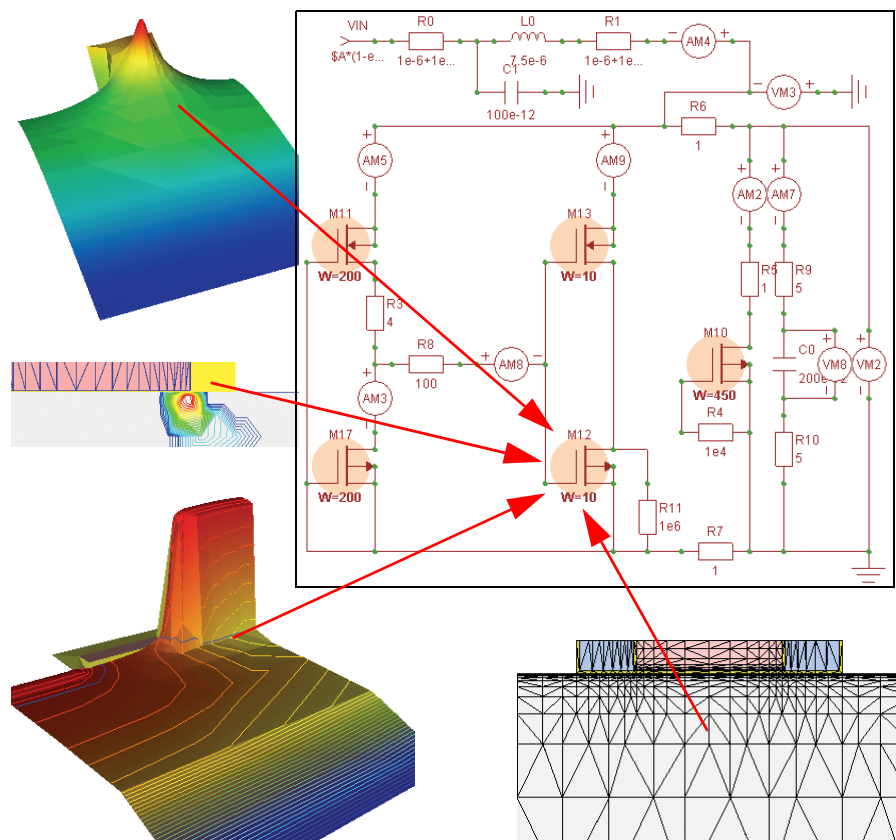


Figure 1. Circuit schematics of ESD protection circuits are entered using the built-in schematic capture tool (above). MOSFETs are simulated on the physical PDE level. Inserts show the temperature distribution (top left), impact ionization rate (center left), electron concentration and electric potential at breakdown (bottom left) and the simulation mesh (bottom right).

## Architecture

SEQUOIA ESD builds upon the solid foundation of SEQUOIA Device Designer, a powerful integrated device analysis and optimization software. The software supports modern techniques such as inverse modeling, which maximize the use of electrically measured data for quantitatively accurate calibrated simulations. SEQUOIA Device Designer and SEQUOIA ESD runs under Windows NT/2000/XP and is a complete self-contained package including all necessary components.

Transient mixed-level simulation captures complex interactions between internal device behavior described on the physical PDE level with other linear and non-linear circuit elements such as resistors, capacitors, etc. Flexible expression evaluation is provided for the description of input excitation waveforms as a function of time and parameter values. Likewise, complex nonlinear circuit elements, such as polysilicon resistors characterized by current saturation effects, are described as analytic expressions through the user interface. All user interaction with the system is through the Graphical User Interface. No editing of simulator files is necessary. Physical accuracy is ensured by inverse modeling techniques, calibrating parameterized PDE-level device to match experimental high-current data such as TLP (Transmission Line Pulsing). An example shown in Figure 2 illustrates excellent accuracy of snapback simulation results for 0.18 micron MOSFET as indicated by near-perfect agreement with TLP data.

The number of PDE-level devices included in a simulation circuit is only limited by the available memory and CPU time. Circuits with 15-20 devices can be easily simulated for ESD stress on a PC. In addition, BSIM3v3-level MOSFETs can be included in simulation circuits for devices not driven into high-voltage/high-current regions of operation, further reducing simulation time and allowing for fast analysis of even larger circuits.

Simulation times for an ESD discharge with 1-10 PDE-level devices are on the order of a few minutes to one hour on a standard PC. Actual CPU times depend on the mesh in PDE-level devices, circuit specifics and input waveform.
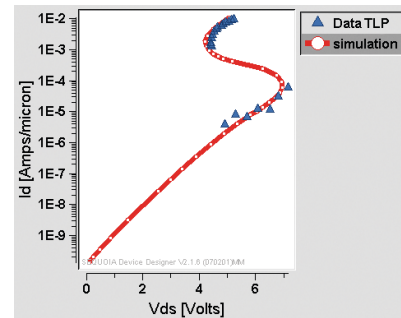


Figure 2. ggMOS snapback simulation (line) and TLP data (symbols).

# Applications

Figure 1 shows schematic of a typical ESD analysis circuit consisting of a grounded-gate MOSFET (M10), an I/O buffer (input: M12/M13, output M17/M11) as well as an HBM stress circuit C1, L0, R1. The protection MOSFET M10 is placed some distance away from the I/O pad. This distance is electrically represented by resistors R6 and R7. If it is too large, MOSFET M12 is at risk of triggering first. Since M12 is a small and not ESD-hardened device, it is not capable of carrying a significant current and must not be allowed to trigger. If M12 triggers, permanent damage to it is likely, such as oxide damage and Vth shift, metallization failure, etc.
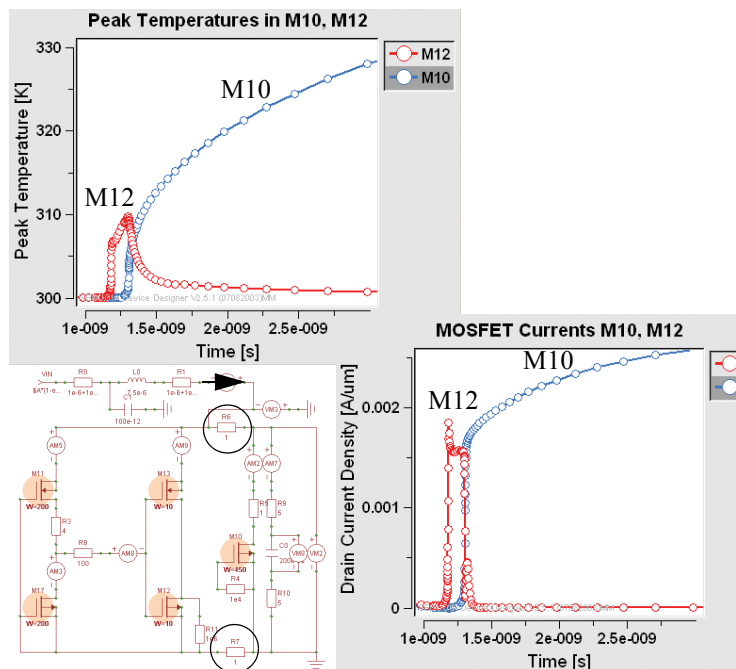


Figure 3. ESD simulation results for the example shown in Figure 1. I/O Buffer MOSFET M12 triggers first due the voltage drop on R6, R7. Damage to M10 is likely due to its small size and non-ESD-hardened design.

Simulation results for a 2kV HBM ESD pulse are shown in Figure 3. Due to the voltage drop on the interconnect R6, R7, I/O buffer MOSFET M12 is exposed to higher voltage than the protection device M10 and therefore triggers first and enters snapback (Figure 3). The protection device M10 triggers with some delay after that with the small MOSFET M12 conducting a significant current until then. This is seen in the MOSFET current densities (Fig. 3 lower right) as well the MOSFET peak temperature plots (Fig. 3 upper left).

Since the I/O Buffer device M12 is not ESD hardened, its triggering indicates a likely reliability problem and must be avoided. This can be accomplished by layout changes, or alternatively by lowering the triggering voltage of the protection device M10.

# For More Information

For more information, to obtain a demonstration version and with all other inquiries please contact SEQUOIA Design Systems at the address below, or your local sales representative.