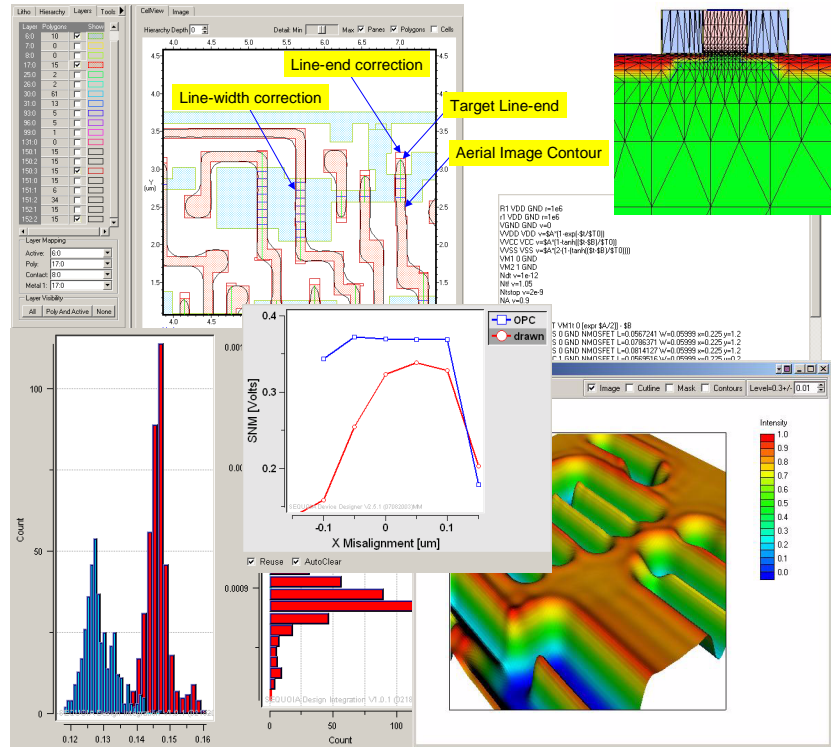


SEQUOIA Cell Designer

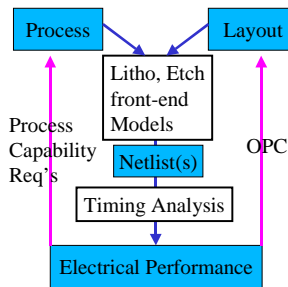
Electrical Performance Verification and Design for Manufacturability (DFM)

Overview.

SEQUOIA Cell Designer is the first tool addressing the core issue of Design for Manufacturability (DFM): predicting the electrical performance of a circuit manufactured on silicon in a specific process. Design data, such as circuit netlist and layout, are combined with process information by physical simulation to predict the electrical circuit performance. Calibrated process simulation accurately predicts the effects of lithography, etch and process variability to obtain physical predictions for circuit performance and yield. SEQUOIA Cell Designer (SCD) links for the first time design and manufacturing to predict circuit electrical performance across process variation in a fully integrated easy-to-use package.



DFM and Verification Flow



Architecture

SEQUOIA Cell Designer provides a complete set of tools integrating a powerful layout database, physical process simulation, accurate front-end device simulation, circuit analysis and statistical yield prediction. Electrical simulation tools used by SCD come from the stable production code used in SEQUOIA Device Designer-ESD, a physical circuit simulation package for mixed-mode circuit-device simulation of ESD protection circuits. Process simulation tools in SCD cover lithography and etch simulation and offer world class algorithms with superior speed and accuracy. Electrical optimization of a cell layout for optimal performance across process variations such as defocus, etch, mask misalignment, etc. can be carried out in minutes. Large cell and full-chip manufacturability analysis is performed in 10-20 hours, depending on process conditions and design size.

For More Information

For more information, to obtain a demonstration version or for other questions please contact SEQUOIA Design Systems, Inc. at the address below.

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