IDENTIFICATION OF ELECTRICAL SIGNATURES OF MASK DEFECTS: A NOVEL PROCEDURE FOR MASK DISPOSITION

by

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ABSTRACT

Inspection and repair are increasingly more important components of the mask building process. Mask writing complexity and time make it necessary to accept plates containing defects such as line protrusions, particles, or voids. These defects are identified by a number of inspection tools, which should make it possible to distinguish between

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"killer" and "nuisance" defects. In the most advanced defect printability studies, a 10% linewidth (CD) variation in critical areas or common process window shrink are used to evaluate defect severity [1]. This emphasizes defect printability for manufacturing rather than product functionality. In this work, we propose a simulation procedure that goes one step further, by evaluating the impact of mask defects on device parameters. It would first define silicon image, followed by the identification of defects that actually degrade device characteristics beyond the limits specified for the product. The procedure uses simulated transistor characteristics based on its geometries and models, with drive and leakage currents used as the qualifying parameters.

INTRODUCTION

Mask defects can occur due to irregularities in the resist process, uneven chrome etching or can be introduced during mask repairs. Implementation of resolution enhancement techniques (optical proximity correction (OPC), phase-shifted masks (PSM) and sub- resolution assist features) bring photomask complexity to the level, where sizes of the legible mask features (serifs, scatter bars) are in the range of minimum detectable defects. As a consequence, the traditional defect assessment scheme, where defect evaluation is based on its size and location is no longer valid [2]. The ultimate question one should ask from now on is, how would mask defects affect the device performance. In this work, we present one way to answer that question. We demonstrate an implementation of a two-stage simulation scheme to identify electrical signatures of mask defects depending on their type, size and location. We have examined the impact of defects on the electrical characteristics and on the parametric yield of the transistor. The defects considered here were similar in size to OPC features on the poly gate and close to the current defect detection capability.

MASK DISPOSITION CRITERIA

The cost of mask inspection and repair is becoming an increasingly large component of the total mask cost [3]. However, while mask defects may degrade device yield beyond acceptable limits, defect detection capability is scaling slower than device geometries. At 130 nm technology node, the Semiconductor Industry Association recommends that the minimum inspectable defect size should be around 100 nm [4], giving a more favorable defect size to CD ratio compared to the future, 70 nm node, with defect size of also about 70 nm [5]. While this requires significant progress compared to the current state of mask defect inspection tools with a pixel size in the range of 125 - 180 nm and a defect detection capability of approximately 200 - 250 nm, it indicates that the traditional mask disposition methodology based on defect size calls for significant enhancement.

In order to expedite mask delivery, it is necessary to design an acceptance process for plates containing defects not impacting product performance. Identification of reticle defects such as line protrusions, particles, or voids is performed by a number of tools or special simulation programs (e.g., Virtual Stepper, nanoprofilometer, AFM) [6]. At the same time, proper tuning of these tools remains a challenge. "Killer" defects need to be distinguished from the "benign" ones, especially ones, which can be termed as "false" or "nuisance". Mask inspection can identify many tens of defects out of which only a few (or few percent) would in fact require to be repaired [6]. Advanced defect qualification tools are already able to identify defect location with respect to other layers such that the defect impact on device parameters (e.g. poly defects with respect to active layer) can be readily evaluated. However, the criterion typically used by the mask inspection tool is simply based on the linewidth (CD) variation by 10% in critical areas. Defect printability is therefore evaluated in terms of integrity of mask fabrication and silicon manufacturing line rather than by the impact of device

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functionality, which is also affected by MOSFET model. Incorrect disposition may translate into either disqualifying a potentially good plate or into many hours wasted on unnecessary repair of tens of "nuisance" errors, taking several minutes each [6]. A significant help in mask qualification is provided by the Virtual Stepper analysis tool, which creates silicon image of the actual mask followed by CD extraction [5]. The use of silicon image usually leads to desensitization of mask inspection as many of deep submicron defects would not print at all, thereby reducing the number of defects to be repaired. However, the 10% CD criterion for silicon image makes the procedure only indirectly useful to evaluate the possible impact of defects on device parameters.

Below, we propose a new procedure of mask defect qualification and reticle disposition. Ordinarily, the impact of defects on MOSFET characteristics cannot be assessed till the device is fabricated on silicon. Our procedure is based on the key criterion such as MOSFET drive or leakage current, with the capability of extension towards evaluating the impact of such defects on product performance. We demonstrate how to provide a direct link between mask defects and transistor current, by a multi-staged simulation. We propose to first define silicon image, in consistence with the initial identification and dismissing of "benign" defects by currently used criteria. This would be followed by focusing on "killer" defects that actually degrade device performance beyond specified limits. In the process, one needs to simulate transistor characteristics based on its geometry as well as device models where drive and leakage currents can be used as the qualifying parameters [8]. As a result, our simulation scheme would help identify the defects that really need to be fixed. One can expect that the mask repair time and cost can be significantly be reduced, perhaps by as much as 50% compared to the mask release using other inspection routines.

MASK DISPOSITION FLOWS

For a 0.12 um process, a critical level reticle such as poly can have a total of about a hundred errors detectable by the inspection tool [6]. That number depends on the inspection routine (die to die or die to database) and tool sensitivity. However, only a few of these errors would impact CDs of the printed pattern, and even fewer of them would affect design performance.

Fig.1 shows a typical mask writing and acceptance flow. Whereas only defects impacting circuit performance should be taken into account, the typical flow based on the 10% CD criterion does not make such distinction possible. Even when the flow is enhanced by silicon image simulation, the correlation to device functionality would still not be available.

In order to account for geometry-dependent transistor performance, device model parameters have to be involved in mask disposition. As discussed, transistor locations on the mask can be identified based on poly/active overlays in the advanced versions of mask inspection flow. However, to extract device parameters from its geometry, it is necessary to know channel doping profiles, effective channel lengths, gate oxide thickness, and junction depths. This information, available from device engineering, is usually not communicated to the mask vendor. In addition, MOSFET geometry is affected by defects located within misalignment budget of active and poly which should be taken into account in device performance evaluation.

In order to keep mask disposition process simple despite added simulation steps, one needs to streamline MOSFET analysis. Firstly, transistor identification, silicon imaging, and parameter extraction can be automated. In this work, we used NTI's IC Workbench with device extractor of Sequoia Design Systems [9] integrated into a system

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where the results of CD analysis are automatically supplied to the device simulator. Secondly, only basic disposition ("reject") parameters such as drive or leakage current (ION, IOFF) should be analyzed, without going into the detailed simulation of MOSFET characteristics. Full MOSFET analysis can be a secondary option, if required. The simulated "reject" device parameters should be then compared to the values specified in the product or technology datasheet.

Fig.2 shows the modified mask qualification flow. The added complexity compared to the flow presented in Fig.1, due to the need of modeling MOSFET characteristics, would be offset by a more accurate qualification of defects resulting in the shorter overall mask write and repair cycle time.

MOSFET ANALYSIS

To evaluate the impact of chrome defects on MOSFET characteristics, we used mask qualification procedure illustrated in Fig.2 for a very dense layout of an SRAM cell for 120 nm technology. We will discuss the impact of different types of errors on poly gate mask on key device parameters such as leakage current IOFF and drive current ION and compare different mask qualification criteria based on 10% margins for chrome CD, gate CD, or MOSFET specs.

Two basic types of defects are protrusion and intrusion of the chrome [5]. Below, we will discuss the impact of protrusions and intrusions ranging from 20x60 nm to 40 X 60 nm @ 1X (160 X 240 nm @ 4X, mask scale) placed along a 120 nm poly gate. Such defects, detected by a sensitive inspection, can be the basis for rejection of the plate. Depending on the different placements of those defects with respect to the FET area, they cause variation of the transistor ION and IOFF. These parameters are calculated by performing statistical analysis of the gate length [7]. Silicon images were simulated assuming a 193 nm stepper with annular illumination; the models for ION and IOFF are based on 120 nm NMOS data.

Fig.3 shows an example of intrusive defects along with their corresponding silicon image of poly gates, overlaid with active area. Depending on the depth and length of the defect as well as on the placement of the defect along the poly, the contour of simulated poly line can significantly deviate from the desired (designed) pattern thereby affecting transistor characteristics.

Fig.4 shows the procedure of MOSFET analysis for mask disposition. In the process, the channel is first divided (discretized) into a number of parallel sections such that its length can be treated as uniform over each section's width. Then, discrete parameters are calculated for each section based on the doping profile etc. and channel length dependent, individual values for IOFF and ION are extracted, as shown in Fig. 5. This is followed by statistical analysis of the extracted data producing also their integrated values for the entire devices. The procedure has been automated and can be easily used for MOSFET evaluation.

Figs. 6 and 7 show the simulated aerial images of poly gates with mask defects located near the edge of the MOSFET channel or directly above it. In general, defects located outside the channel area have only minimal impact on gate CD, thus showing that mask qualification procedure should be sensitive to defect location.

Fig.8 shows the ION and IOFF values extracted based on MOSFET channel geometries, as illustrated in Fig.6 and 7. As expected, the off-gate defects (Fig.6) would barely change device characteristics, regardless of their sizes. All the masks with such defects should be then accepted without repair. On the other hand, on-gate defects are shown to cause more substantial variations of drive current (within the assumed MOSFET model). The largest ones would make it necessary to have the plate repaired.

Table 1 shows a comparison of mask acceptance criteria based on CD and MOSFET analysis. As an

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example, a chrome extrusion of 40 nm over a chrome line of 120 nm would produce 11 nm extrusion of silicon image. Considering now mask acceptance criteria, the plate would be subject to rejection, as the chrome line width is by 30% larger than nominal. At the same time, based on silicon image simulation, the mask would be subject to repair, as the gate CD variation was only about 10%. However, the simulated ION show merely a 0.7% reduction which, depending on MOSFET acceptance criteria, could eliminate the need to retouch the defect (the IOFF was also reduced, which was in agreement with device spec).

Mask intrusions are, according to the simulation, impacting silicon image much stronger than the extrusions. Again, according to the chrome CD criteria, no intrusion from the ones listed in Table 1 would be allowed; any of them would cause mask rejection. Using 10% silicon image CD criterion, only the smallest intrusion from the listed ones would be accepted for repair. According to the procedure proposed here, the actual mask acceptance would be determined by the MOSFET leakage tolerance. One possible criterion would be increase of log 10(IOFF) by 10% (which corresponds to IOFF increase by no more than 25%. One should note here that the CD reduction by 10% over the entire channel width can lead to the increase in IOFF by an order of magnitude). In such case, only the largest defect size would be unacceptable for mask acceptance without repair; otherwise, the plate would only need a minor touchup.

SUMMARY

In summary, we proposed a novel, efficient mask qualification procedure that makes it possible to identify and focus on repairing only defects important from the device performance standpoint. The procedure, based on a two-stage simulation, can be included into the standard mask qualification process flow. We propose to use the simulated electrical signatures of mask defects to improve the mask defect inspection process. Optical and electrical simulation can be used to define more accurately the maximum allowed size and critical location of mask defects. It can potentially eliminate a large number of unnecessary repair operations thereby reducing mask cost and improving the cycle time. In this work, we demonstrated the procedure on poly gate level. The calculations, done for several different defect sizes, showed that the impact of chrome CD variation is significantly higher for intrusions than for extrusions of identical sizes. Depending on defect location, the impact on FET parameters was within 10% CD variation or outside of that limit. The CD variation criterion did not always correlate with device performance as measured by the drive or leakage current.

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Figure 1: An example of advanced procedure to qualify mask defects and disposition of critical mask layers using simulation of silicon image. An important parameter is the allowed process window reduction (x %). Process window calculation is based on the exposure/defocus matrix simulated based on the mask.

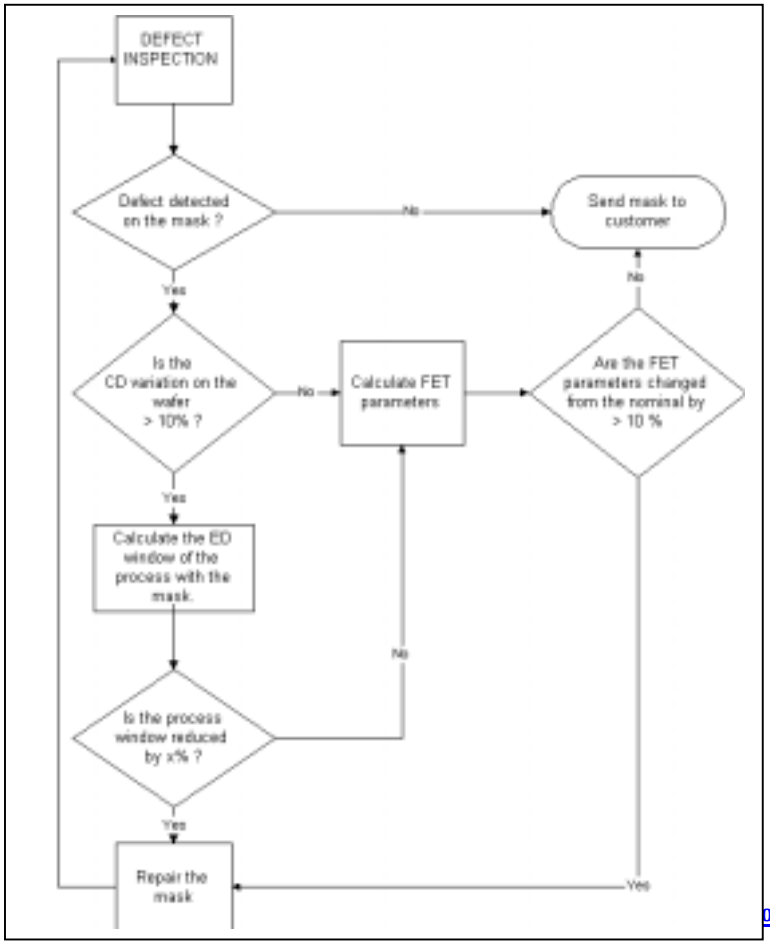

Figure 2: The novel mask qualification procedure proposed in this work. In addition to the disposition criteria proposed in Fig.1, it would also involve an additional one – the allowed change of MOSFET parameters (here, by 10 %).

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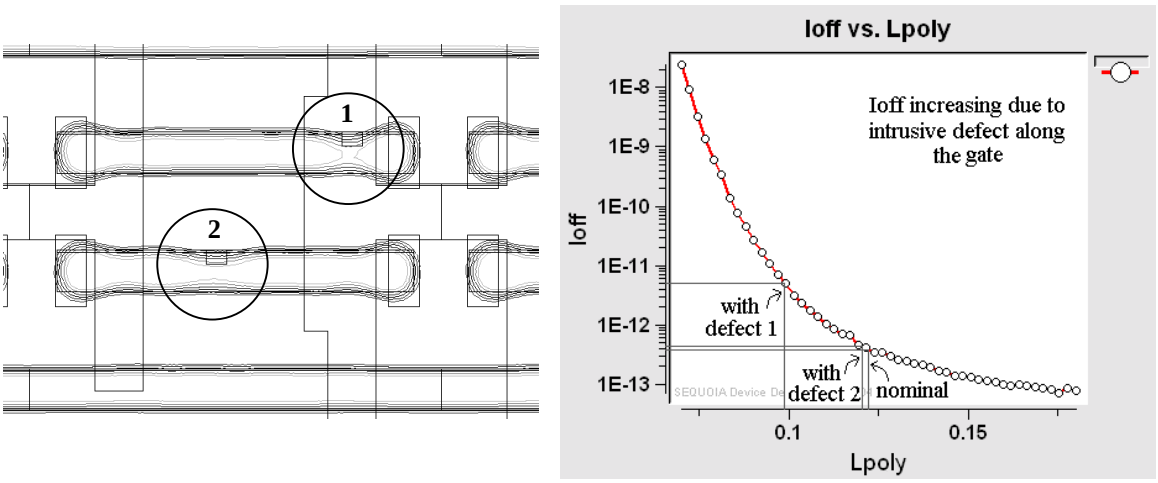

Figure 3: Left: An overlay of drawn diffusion and poly layers and simulated silicon patterns of poly gates, showing examples of intrusions and extrusions placed in different locations (1: over the MOSFET channel, 2: between two MOSFETs). Right: An example of MOSFET analysis based on channel length dependence of IOFF current, with and without defects, as marked on the picture on the left.

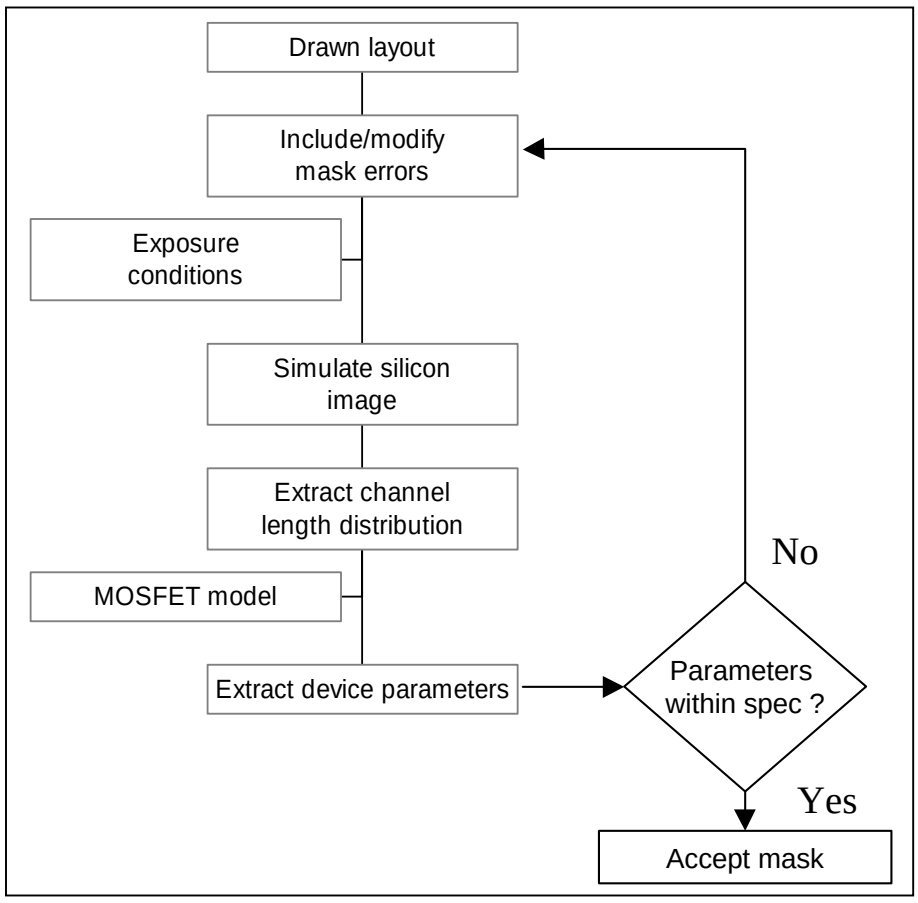

Figure 4: An integrated mask defect simulation and MOSFET extraction scheme used in this work, allowing mask qualification as proposed in Fig.2.

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	20_60_med_delta
Low	-13.66
High	-13.4
BarWidth	0.008639
Samples	40.0
Mean	-13.46
Sigma	0.05519
Low Spec	-14.617
High Spec	-11.959
Below Spec %	0.0%
Above Spec %	0.0%
Yield %	100.0%

Figure 5: Output from device simulator [8] showing geometry-dependent MOSFET IOFF parameters.

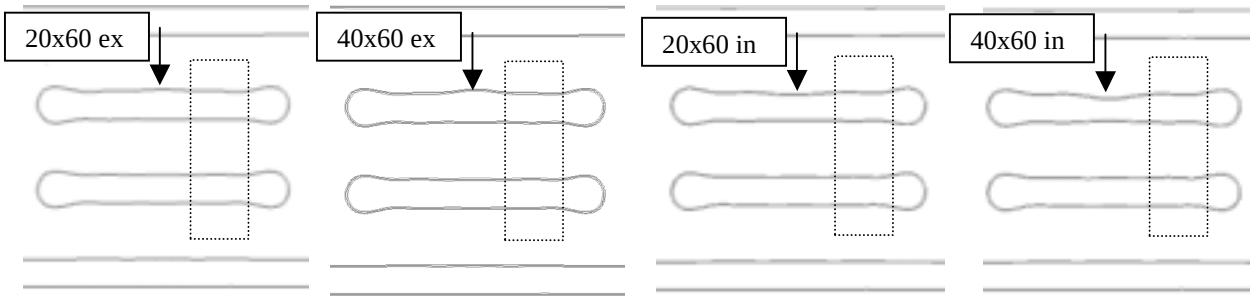

Figure 6: Aerial images of poly gates simulated from the masks with different types of defects: protrusions (marked "ex") and intrusions (marked "in"), with two different sizes (x and y dimensions in nm), situated away from the MOSFET channel (marked by the dotted line).

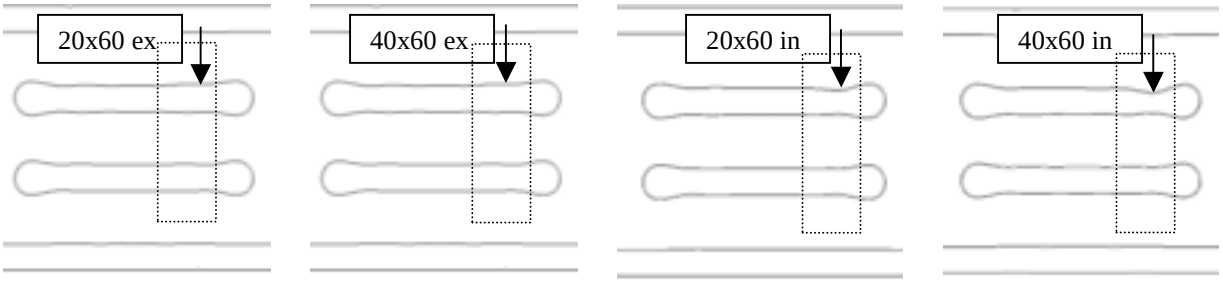

Figure 7: Aerial images of poly gates simulated from the masks as in Fig.6, but situated directly over the MOSFET channel (marked by the dotted line).

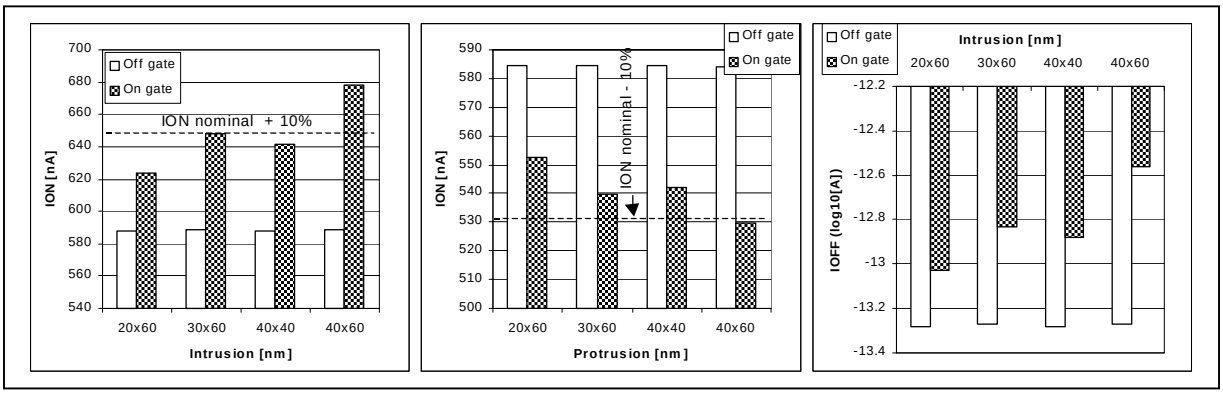

Figure 8: Simulated ION and IOFF for the different mask defect sizes and locations.

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Defect		**Disposition according to 10 % criteria**			
Type	**Size**	Mask CD	Silicon line CD	MOSFET Log IOFF	MOSFET ION
Protrusion	20 x 60	Fix	Ship	Ship	Ship
	30 x 60	Fix	Ship	Ship	Ship
	40 x 40	**Reject**	Ship	Ship	Ship
	40 x 60	**Reject**	Fix	Ship	Fix
Intrusion	20 x 60	Fix	Ship	Ship	Ship
	30 x 60	Fix	Fix	Ship	Ship
	40 x 40	**Reject**	Fix	Ship	Ship
	40 x 60	**Reject**	**Reject**	Fix	Fix

Table 1: Mask disposition depending on defect acceptance criteria.

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