Design and Simulation of ESD-Resistant ICs

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***Abstract*—Robustness of modern ICs during system assembly and normal operation requires that protection circuits are built-in to prevent damage to internal circuit elements due to Electrostatic Discharge events (ESD), which can inject substantial energy into the chip. ESD protection as well as protection against other damaging events, such as latchup, is highly dependent on chip architecture and circuit design, electrical properties of interconnects and parasitic devices, and of course device design and semiconductor process technology.**

Design of built-in protection circuitry is by nature analog and must consider layout specifics. It must also include accurate models for the physical devices, both desired and parasitic. Details of process technology determine the behavior of protection devices as well as damage thresholds of the protected circuits, while their circuit configuration and specifics, such as device and interconnect sizing ultimately determine whether the circuit will survive the ESD event. Mixed-level circuit-device simulation is used with great effect for these design tasks, with Finite Element/Difference models deployed for critical elements, such as MOSFETs, diodes, SCRs, etc. where needed, while conventional SPICE compact models are used elsewhere to create a complete circuit model of the entire damaging event. This approach brings the physical accuracy of partial differential equation models to the modeling of circuits.

A review of the technique, some important practical aspects and applications to ESD design are presented and industrial examples are discussed in this paper. Wider applications of the technique are touched upon, including simulation of practically important power circuits under realistic load conditions, latchup and other effects, which all by their nature require an in-depth physical analysis beyond the scope of SPICE compact models.

***Index Terms*—ESD, Latchup, Power Devices, Analog Design, Physical Design, Simulation, TCAD**

I. Introduction

Effective built-in protection from Electrostatic Discharge (ESD) events is essential for modern integrated circuits. Their high sensitivity to small amounts of charge is the inevitable consequence of small device geometries, unable to absorb even small amounts of charge without suffering damage due to overheating, metal failure, oxide failure, etc. ESD events must therefore be properly anticipated and protection circuits must be included on chips to divert and dissipate incoming discharge energy away from sensitive elements.

On-chip ESD protection is typically tested with and therefore designed for one or several of the standard ESD tests. In particular, three types of ESD tests are common and are usually targeted. All can be modeled by a simple RLC circuit with specific circuit element values connected to the Device Under Test (DUT), such as an I/O pin of a chip. The RLC circuit contains a pre-charged capacitor, which is discharged into the DUT through a series resistor and a series inductor as shown in Fig. 1. Typical RLC values for common ESD tests are shown in Table I. These ESD test types are:

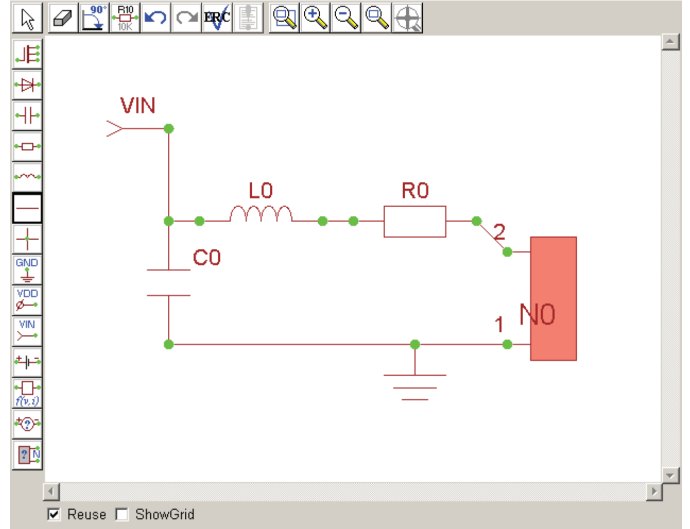

Fig. 1. ESD subcircuit describing stress on device I/O pads. The capacitor C0 is pre-charged to a specified voltage, then discharged into the DUT marked as N0 through the inductor L0 and resistor R0. RLC values are shown in Table I for standard chip-level tests.

TABLE I
Standard chip-level ESD tests and typical values of the ESD stress RLC sub-circuit in Fig. 1

ESD Test	C	R_{series}	L_{series}	typical stress level
HBM	100pF	$1.5k\Omega$	$1\mu H$	2000V
MM	200pF	5Ω	$0.6\mu H$	100V
CDM	2.5pF	30Ω	$20nH$	500V

- HBM - Human Body Model is intended to mimic a human operator touching a chip pin, typically during assembly. This discharge is characterized by a relatively large series resistor and is comparatively slow. The discharge current has the shape of a pulse with a peak value of ~1.3A for a 2kV discharge, rise time ~10ns and fall time ~100ns. HBM is slow enough for significant heat to build up in ESD protection devices. Typical failure modes include local overheating and metalization failure, which usually occurs first due to lower melting temperature of aluminum metalization than that of silicon.
- MM - Machine Model represents a more severe discharge event, where a charged metal part (typically part of an automatic assembly machine) touches a chip pin. This is

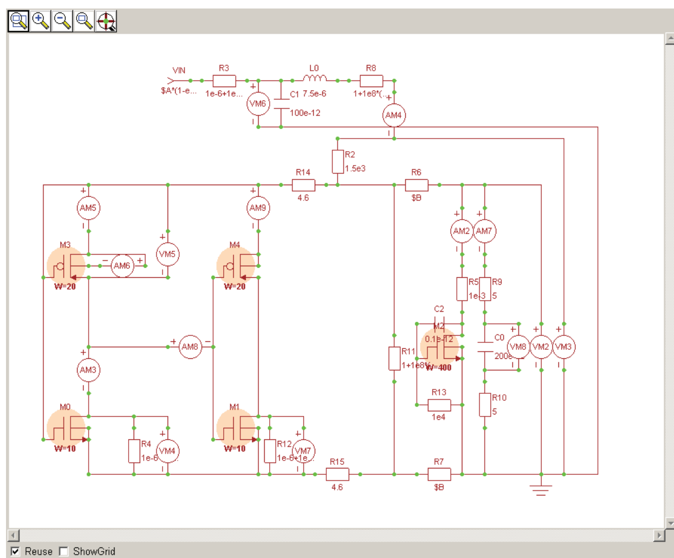

Fig. 2. ESD simulation example incuding a discharge sub-circuit C1L0R8 like the one shown in Fig. 1, a large MOSFET M2 used as an ESD protection device and two CMOS inverters representing I/O buffer circuits. Interconnect parasitics are crucial and are included as resistors R6,R7.

a high frequency oscillatory discharge event due to its low series resistance. The capacitance of the machine is large and the discharge energy is relatively high. Heating and damage can result. Failures can show local overheating as well as current or voltage over-stress.

- CDM - Charged Device Model is the fastest ESD discharge event and the most difficult one to test for and model. CDM is designed to mimic a pre-charged chip touching a grounded metal part. The charged capacitance is small, but so are the inductance and resistance. A CDM discharge therefore typically results in very fast transients (<1ns) and high oscillating currents of up to $10 - 20$ Amps. Current flows in internal chip circuits between different circuit blocks and may require local protection. Typical damage caused by CDM includes metal failure due to current over-stress and oxide failure due to voltage over-stress. Failure is not always limited to I/O circuits and may occur elsewhere, in particular in circuits interconnecting various circuit blocks. Overheating is less common with this fast event.

Simulation capabilities are key to effective design of ESD-robust integrated circuits as well as for the analysis of ESD failures in manufactured chips. As evident from the above description of standard ESD tests, accurate simulation must include relevant portions of the DUT (Device Under Test) such as protection devices, circuits or parts of circuits subject to ESD stress, and importantly also on-chip parasitics such as interconnect resistances, capacitances of circuit blocks, etc.

As an example Fig. 2 shows a typical circuit used to simulate the behavior of on-chip ESD protection under HBM/MM/CDM stress conditions. A discharge sub-circuit, as shown in Fig. 1, attached to the I/O pad is included, as well as a grounded-gate MOSFET protection device and parts of the I/O buffer. Parasitics, such as line resistances and capacitances are key for this simulation and greatly influence the outcome and accuracy of the simulation.

II. ESD as a Technology-Specific Circuit Issue

From the example shown in Fig. 2 it is obvious that much more than just the ESD protection device is involved in an ESD event. It is rather an entire circuit, which of course includes the protection device but also other components. The values of parasitics, in particular interconnect resistances and capacitances of on-chip circuit blocks are key to the current flows and resulting stress on the circuit components. Without a sufficiently complete and accurate model for the entire relevant circuit it is impossible to properly design ESD protection or analyze its performance.

The capabilities of the protection device itself are determined by its physical characteristics, such as dimensions and process technology. For example, if a grounded-gate MOSFET is used, its triggering voltage Vt1 will be determined by its gate length, oxide thickness, channel doping and junction profile. Its holding voltage will be controlled by the well profile and placement of well contacts, while the failure current is a function of device width, metalization, etc. An FEM-level model of a MOSFET may be discretized with a mesh as the one shown in Fig. 3. In some cases more complex models may be used, for example when the influence of substrate coupling on the performance of multi-finger MOSFETs is of importance [13]. Of course, all this will be different if for example an SCR is used instead of a MOSFET.

Physical simulation using the Finite Element/Difference Method (FEM/FDM) provides a physically accurate model of the protection device or devices. Electrical properties of such devices such as Vt1 result from the specified device geometry and built-in physical models used to describe effects such as impact ionization, velocity saturation, tunneling and many others.

We therefore make the observation that while ESD design must involve knowledge and understanding of process technology, the primary issues in ESD design present themselves at the circuit level and must be addressed there. As an example, means to improve ESD protection usually include increasing the size of the protection device to reduce its impedance or reducing the distance between the I/O pad and protection device to reduce the interconnect resistance. On the other hand, process technology is typically frozen at the time of ESD design or determined by other considerations and is not usually changed solely for ESD performance reasons.

III. Mixed-Level Circuit-Device Simulation

A. Device Simulation, Circuit Simulation, and Mixed-Mode

1) Device Simulation: Transport of charged carriers in semiconductors is described by a well-known set of three (or four, if self-heating due to current flow is of importance) second-order partial differential equations: Poisson's equation (1) and two carrier continuity equations for electrons eq. (2)

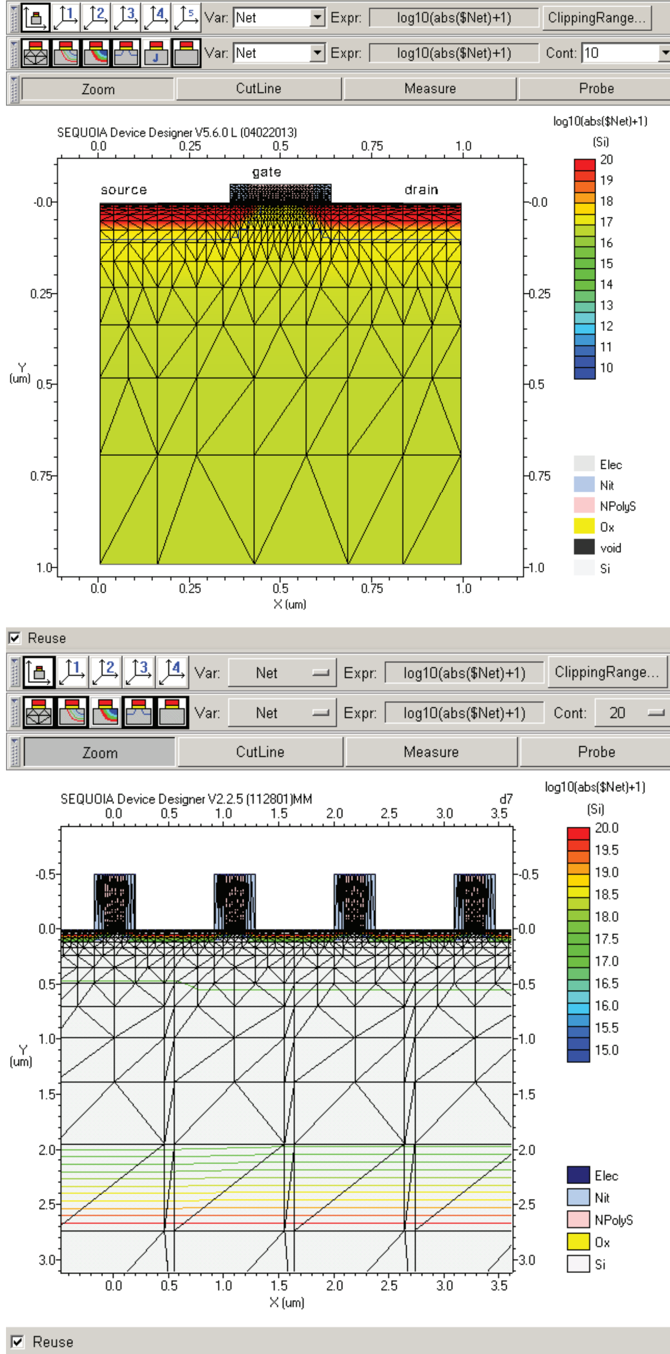

Fig. 3. Example FEM models of ESD protection device: a 2D mesh and doping contours of a MOSFET (above), simulation mesh and structure of a multi-finger MOSFET with four gates as discussed in [13].

and holes eq. (3). For some applications including slower ESD events, power devices, latchup and reliability it is also necessary to consider device self-heating due to current flow eq. (4), see for example [10].

This system is highly nonlinear, in particular the drift terms in both current continuity equations are products of carrier concentrations times electric field. The electron and hole currents $\vec{J_n}, \vec{J_p}$ are a sensitive balance of large and usually opposing drift- and diffusion currents, which can cause loss of accuracy with standard solution methods. Narrow boundary layers (known as depletion or inversion layers) occur in nearly all devices at pn-junctions and channels and are difficult to resolve with standard discretization and meshing techniques. The solution of these equations is challenging and requires specialized treatment. [1]

$$\nabla\epsilon\nabla\psi = q(n - p - N_D + N_A) \tag{1}$$

$$\nabla \cdot \frac{\vec{J_n}}{-q} = \frac{\partial n}{\partial t} + R - G \tag{2}$$

$$\nabla \cdot \frac{\vec{J_p}}{q} = \frac{\partial p}{\partial t} + R - G \tag{3}$$

$$\nabla\kappa\nabla T = \rho\frac{\partial T}{\partial t} - (\vec{J_n} + \vec{J_p}) \cdot \vec{E} \tag{4}$$

with electron and hole current vectors defined as:

$$\vec{J_n} = q\mu_n(-n\nabla\psi + kT/q\nabla n)$$
$$\vec{J_p} = q\mu_p(-p\nabla\psi - kT/q\nabla p)$$

With very few exceptions, practical simulation of semiconductor devices on the level of partial differential equations is based on the pioneering Scharfetter-Gummel discretization [1]. This discretization is based on the analytical solution of the one-dimensional semiconductor equations, possible under a few reasonable assumptions. Multi-dimensional extensions of the scheme were achieved using the box integration method or finite volume method. In comparison to more standard Finite Element discretization with linear shape functions, or other mathematical discretization techniques, such as for example [8], the Scharfetter-Gummel method can work with generally much coarser discretization girds, while maintaining good accuracy and, importantly, current conservation. Grid generation is in general of paramount importance for practical applications. Poor choice of grid may cause convergence problems, accuracy problems or both. A well-designed good quality grid is key to achieving fast simulations and good accuracy and is usually the single most important aspect of device simulation over which the user has some control [11].

Two-dimensional device simulation was introduced in the early 80-ties with packages like MINIMOS from University

[1] In the above equations ψ, n, p, T are the electrostatic potential, electron, hole concentrations and lattice temperature, N_D, N_A are the donor and acceptor concentrations, μ_n, μ_p are electron and hole mobilities, κ is the thermal conductivity, ρ is the specific heat capacitance, R, G are recombination and generation rates, q is the electron charge and kT/q is the thermal voltage.

of Vienna [2] and PISCES from Stanford University [3]. In particular PISCES and its derivatives became widely used in the industry and academia due to its flexible triangular discretization grid and suitability for a range of semiconductor devices including MOS, bipolar, power, etc. Commercial device simulation tools based on PISCES II [6] were developed and sold by TMA and Silvaco and became standard industrial device simulation tools in the 90-ties.

2) Circuit Simulation: Circuit simulation work started at about the same time as device simulation, although with a much lower computational load it became practical somewhat earlier with the release of SPICE (Simulation Program with Integrated Circuit Emphasis) from UC Berkeley [4], [5]. SPICE calculates the steady-state or transient solution of current balance equations (Kirchhoff's current equations) at each node of the circuit. These equations are physically equivalent to a lumped representation of the microscopic-level current continuity equations eq. (2), eq. (3). Nonlinear circuit elements, such as transistors, diodes, etc. are represented by analytical so-called compact models. Accuracy is achieved by adjusting parameters to match measured data, a process known as parameter extraction. Fast model evaluation is achieved at the cost of some loss of physical scalability and predictive ability. Because of the high evaluation speed of analytical models used in circuit simulation, relatively large circuits with thousands of transistors and other elements can be modeled.

Since all devices are embedded in circuits, the goal of any simulation is ultimately to predict how the circuit will behave. Device simulation work addressed this by extracting certain electrical metrics of device behavior, such as gate curves, drain curves, subthreshold slope, threshold voltage, breakdown voltage, etc. These metrics were then used to assess device behavior when it was used in a circuit. In some cases entire compact models are extracted from device simulation results and passed on to a SPICE-type circuit simulation.

The circuit simulation approach is limited in two important aspects:

- when complex physical effects not covered by compact models are important during operation of the device. Examples include impact ionization (avalanche breakdown) in snapback-type ESD protection devices or power devices. Other examples are device types which are difficult to model analytically due to their complexity, such as DMOS, IGBT, SCR, etc.
- use of analytical models with fitted coefficients makes it less likely that accuracy is preserved with changes in layout or process technology. Since doping information and device geometry is not considered directly, while it may be possible to create a model for a particular device and fit it to measured data, it may only be usable for one specific configuration. As an example, it is possible to create analytical models for certain types of snapback devices, including grounded-gate MOSFETs or SCRs. Such models however do not scale well with contact spacing and placement, gate length, oxide thickness, source/drain junction profiles, etc. and are not well suited for design optimization where such parameters may be considered.

3) Mixed-Mode Simulation: A natural solution is presented by a combination of device and circuit simulation, where device-level models are embedded in a circuit. This addresses limitations of both sides by adding a realistic circuit environment to devices and at same time by adding physically accurate and scalable device models to circuits. The price for this is increased computational effort. Replacing compact analytical models with a discretized Finite Element/Difference solution of a system of nonlinear partial differential equations comes at the cost of adding thousands of equations to the system for each device-level model. As a result, mixed-mode simulations are an effective tool for accurate physical simulation of circuits of limited size, typically up to 10-20 active devices.

ESD analysis happens to be very well suited for mixed-mode simulation, since compact models are typically unable to handle relevant physical effects (such as impact ionization and snapback) and on the other hand the circuit size necessary for analysis is small enough for mixed-mode simulation, typically $< 10 - 15$ or fewer devices are sufficient.

Mixed-level circuit-device simulation was first developed in the late 80-ties, with the most effective and successful approach being the simultaneous coupled solution of device and circuit equations in a single system, demonstrated by Rollins and Choma [7]. This approach places all equations into one large system as shown in Fig. 4, including the equations for FEM-level devices, conventional circuit nodal equations as well as coupling terms between them. The equations are then solved iteratively using Newton's method and linear solvers.

The linearized system is sparse and well-suited for sparse matrix solution methods, both direct LU-decomposition (Gaussian elimination) and iterative methods. Coupling between devices is only via the circuit (blocks along the bottom row and right columns of the matrix), so that matrix fill-in is well contained. Other architectures relying on black-box coupling of a circuit simulator, such as [4], and a device simulator, such as [3], were also tried but proved less effective due to convergence issues caused by severe nonlinearities, in particular in device equations.

B. Calibration and Accuracy for ESD Design

Not explicitly shown in eqs. (1) – (4) are a large number of so-called "physical models" used to describe the dependence of coefficients, such as mobility $\mu_{n/p}$, recombination/generation R, G and others on impurity profiles, properties of interface surfaces, electric field strength, mobile carrier concentrations, local temperatures, etc. Some of these models are well characterized for a range of semiconductor technologies and reliable coefficients are available and have been used for many years. Others vary more strongly with specific technology and have to be occasionally verified with measurements and calibrated.

Importantly, device or mixed-mode simulation assumes knowledge of device structures and doping profiles. In reality

$$
\begin{bmatrix}
D_0 & 0 & 0 & \dots & D_{0,C} \\
0 & D_1 & 0 & \dots & D_{1,C} \\
0 & 0 & D_2 & \dots & D_{2,C} \\
\vdots & \vdots & \vdots & \ddots & \vdots \\
C_{D_0} & C_{D_1} & C_{D_2} & \dots & C
\end{bmatrix}
$$

Fig. 4. Mixed-mode system matrix (Jacobian) structure. Diagonal terms D_i are the system matrices for each one of the devices, C is the matrix representing the circuit, and C_{D_i}, $D_{i,C}$ are the coupling terms describing the connections between the circuit and device electrodes. The location of coupling terms, along the bottom row and right column of the matrix only, means that fill-in during LU matrix decomposition is limited, resulting in good performance of sparse algorithms.

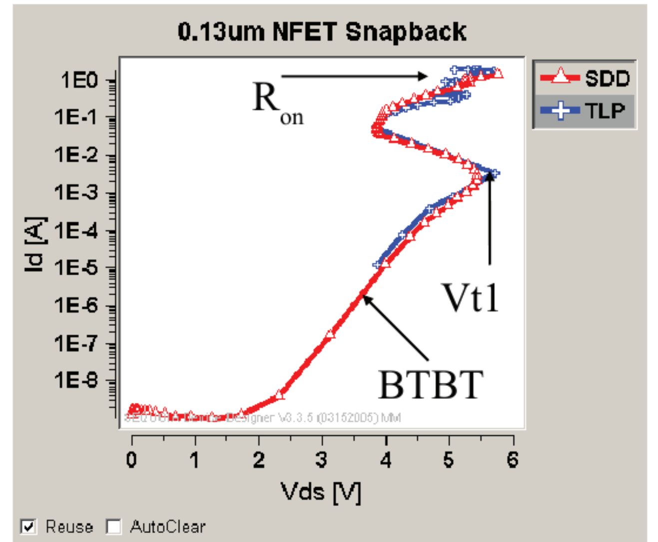

Fig. 5. TLP data (blue crosses) for a grounded-gate MOSFET in 130nm technology and simulation results after calibration (red triangles). An excellent match of the entire curve is seen for both pre- and post-breakdown behavior. Limited accuracy of TLP at low current levels and some noise at high currents (probably caused by multi-finger effects [13]) are visible.

this information is usually obtained from process simulation (in some cases also measurements) and is not without uncertainty itself. To validate accuracy it is therefore in general necessary to calibrate ESD simulations to relevant measurements. In some cases this calibration process can be also used to finalize some device geometry or doping profile details, a technique known as inverse modeling.

Two types of electrical tests are common for ESD purposes: a) ESD testing which emulates actual ESD stress as defined in accepted ESD standards Fig. 1 and b) TLP (Transmission Line Pulse) testing, which uses a pre-charged long transmission line to create a constant current pulse of short duration, typically 100ns. The idea is to keep the pulse short enough to avoid self-heating in the device under test and measure the voltage drop corresponding to the injected current. By applying successively increasing pre-charge values to the transmission line, an entire isothermal IV curve up to device failure point is obtained (TLP curve). Simulation can then be compared to the TLP curve and checked for matching. If significant discrepancies are observed, the device structure, doping profiles or model coefficients (usually in this order) can be tuned. An example is shown in Fig. 5 for 130nm technology. Each data point on the TLP curve (blue crosses) is a separate measurement.

C. Numerics and Performance

As pointed out above, mixed-mode circuit-device simulation is different from conventional SPICE-type circuit simulation in that more physical but also more computationally demanding models for devices are included. The cost for the improved physical accuracy is therefore higher CPU time and memory for a given circuit size, or smaller maximum practical circuits than possible with SPICE. As indicated by Fig. 4, the computational cost of using a FEM device model is determined by the sub-matrix D_i and coupling terms, which for a device mesh with N nodes adds $3N$ (or $4N$ if thermal effects are included) unknowns to the system, one value for each of ψ, n, p, T at each node of the mesh. Obviously, mixed-mode simulation as all computing has greatly benefited from Moore's law and faster computers over the past decades and much larger circuits are easily possible now than was the case at the time when mixed-mode simulation was first proposed.

Recent advances in CPU technology have been more heavily focused on multi-core architectures and less on raw CPU clocks. As a result, parallelization has become increasingly important to fully utilize modern CPUs. Since standard desktop CPUs can now have 8 or more cores, very high performance can be obtained with parallelization. As a result, ESD simulations of HBM/MM/CDM events in relatively complex circuits have been successfully performed in minutes on standard desktop PCs.

As an example, Section IV discusses analysis results of an I/O circuit with 7 FEM-level devices and 3.5 minutes simulation time on a quad-core machine for a full transient 2kV HBM discharge. This is fast enough to run many design iterations of an ESD circuit in a few hours. Mixed-mode circuit-device simulation can be currently used as a practical design tool for circuits with up to 10-20 FEM-level devices with reasonably fine discretization grids. Of course, in most cases a much smaller circuit with perhaps 3-4 devices is sufficient for ESD design. Such circuits are simulated relatively quickly as shown in Tables III-C, III-C for a 7-device circuit [12]. Applications with non-standard devices, such as latchup or power devices, which in general require larger FEM grids, are also been routinely carried out without the use of specialized computing equipment as discussed in Section V.

With standard desktop computer typically configured with several GB of memory (and up to 8-16GB is common), sufficient memory is usually available so that the CPU time rather than memory is the limiting factor. Except for 3D

TABLE II
ESD SIMULATION RUN TIMES FOR A CIRCUIT WITH 7 FEM-LEVEL DEVICES ON A SINGLE-CORE 2GHZ MACHINE[12].

ESD Test	CPU Time (single core)
HBM 2kV isothermal T=300K	9.1min
HBM 2kV with self-heating	11min
MM 100V	36min
CDM 500V	15min

TABLE III
MULTI-CORE SPEEDUP IN AN HBM BENCHMARK EXAMPLE [12].

	1X	2X	4X
CPU time	9.1min	6.3min	3.5min
speedup	1	1.4X	2.5X

simulations, which are not usually performed for ESD circuits for a number of reasons, direct linear solvers are used. As usual, in comparison to iterative solvers, better convergence and lower CPU time are typically achieved with direct solvers at the cost of higher memory use.

IV. APPLICATION: I/O BUFFER WITH ON-CHIP ESD PROTECTION

We now turn towards practical applications of the mixed-mode simulation technique. Fig. 6 shows an ESD simulation circuit used in real-life industrial work. All components involved in an ESD event are included in the circuit:

1) the ESD stress sub-circuit
2) a protection circuit, in this case a large MOSFET with diodes used to direct the discharge current from the I/O pad towards the power supply which contains the protection device
3) protected I/O buffer represented by two CMOS inverters
4) interconnect parasitics, such as resistances of metal lines connecting the I/O pad to the power supply, as well as the capacitance of the protected circuit block represented by C5

This simulation setup allows the ESD design engineer to optimize the circuit considering a number of key issues including:

- Design of the diode circuit D0, D1 including diode sizing and layout to redirect ESD current towards the protection device M2. Diode doping profiles are determined by process technology and are not usually modified during ESD design.
- Performance and necessary sizing of the main protection device M2. This is a function of process technology used to manufacture this device (doping profiles, oxide thickness, etc.), as well as layout (gate length, contact spacings) and, importantly, the protected circuit and its parasitics: contact/via resistances, metal line resistances, capacitances, etc. Mixed-mode simulation results provide information about the performance of this circuit under all of the above conditions and thus allow numerical experiments to find an optimal configuration.
- Requirements on the interconnect (maximum allowable resistance) used to conduct ESD stress current from the I/O pad to the protection device to keep the IR voltage drop low enough for effective protection.
- Potential triggering of I/O buffer devices. If such triggering occurs, permanent damage to these devices is possible (very likely for salicided devices) and can be considered indication of ESD failure.

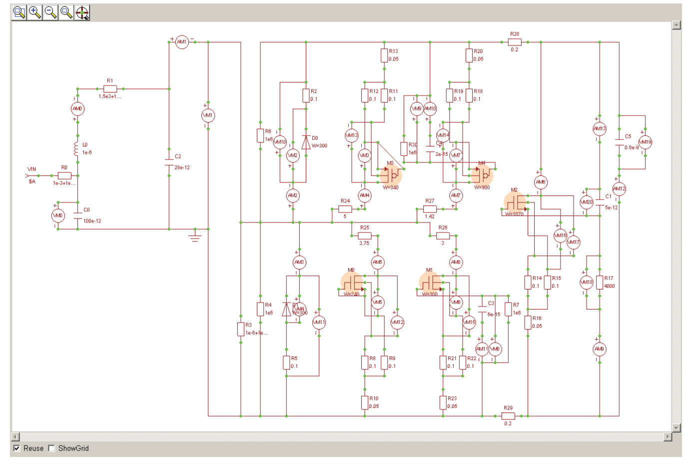

Fig. 6. An industrial ESD simulation: I/O buffer with on-chip ESD protection. External ESD stress is modeled using the RLC sub-circuit (left), protection diodes D0, D1 direct the incoming ESD current towards the protection device M2 located in the power supply (right), I/O buffer circuits are represented by two CMOS inverters M0,M3 and M1,M4. Interconnects are as usual of crucial importance and are represented by their resistances. Capacitance of the circuit block attached to M2 is also important and is modeled by C5.

The circuit shown in Fig. 6 includes a total of 7 FEM-level devices: two diodes D0, D1 and five MOSFETs – one large protection device and four I/O buffer driver devices. The diodes include STI regions and are discretized with $\sim$600 mesh nodes each. Fig. 7 shows one of the diodes (D0) in on-state during an HBM discharge, the electron concentration is high throughout the device indicating high conductivity, the current flows around the isolation region and reaches deep into the substrate. MOSFETs are discretized with 400-800 nodes depending on the device. During operation of the protection N-MOSFET device some internal heating is visible in the temperature contour/color fill plot in Fig. 8. Peak heating occurs in the drain junction due to the high electric field there. Peak impact ionization occurs at the same location. The current flow lines clearly show leakage induced by impact ionization with current flow downward into the substrate.

Various types of ESD stress are modeled using ESD sub-circuit values as shown in Table I. Different RLC values of the stress subcircuit emulate different types of ESD stress as discussed in Section I. Depending on the type of ESD stress and stress level the current and voltage waveforms will be totally different and may cause damage and failure at different locations and of different type. Therefore several ESD tests

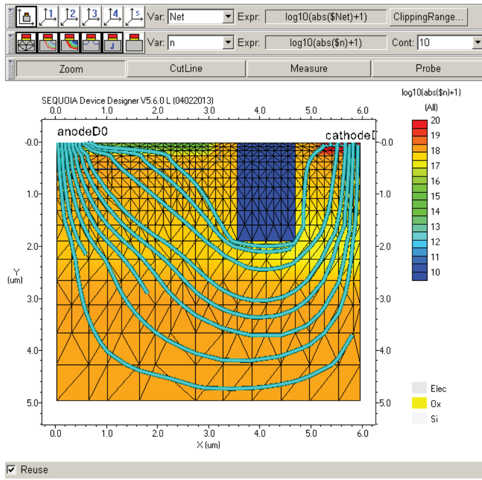

Fig. 7. Diode structure and mesh used for I/O buffer ESD simulation. A total of 591 mesh nodes are used for discretization. The device is in on-state, its electron concentration is shown as color contours, current flow is shown as thick blue tubes. The current flows around the shallow trench isolation (STI) region.

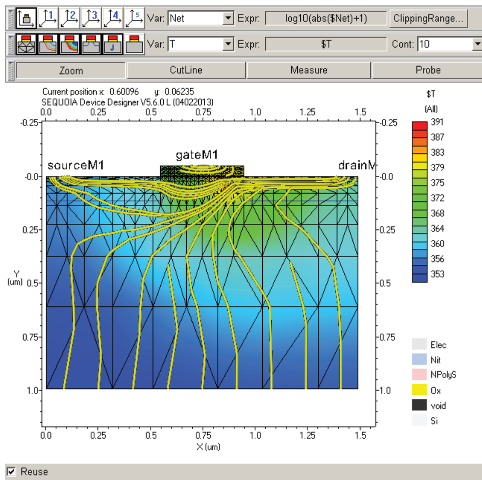

Fig. 8. MOSFET structure and mesh used for I/O buffer ESD simulation. A total of 421 mesh nodes are used for discretization. The device is conducting some current in its channel, there is also significant impact ionization generation of electron-hole pairs in the drain junction visible as a substrate current (hole current from the point of generation down into the substrate). Local temperature is shown as color contours, current flow is shown as thick yellow tubes. Peak temperature occurs at the drain junction and is ~391K in this case.

may be specified as acceptance criteria by a chip customer and must therefore be considered by the designer. For each type of ESD stress simulation shows current and voltage waveforms and is used to predict levels of stress which will occur in the circuit. This is shown by the time evolution of the I/O pad potential in Fig. 9.

The protection circuit works well in all three cases, keeping the maximum pad potential under 7V. This is enough to protect thin oxides from voltage overstress in this case. Clear differences are seen in the shape of pad potential waveforms: HBM is relatively slow peaking at around 100ns, MM shows

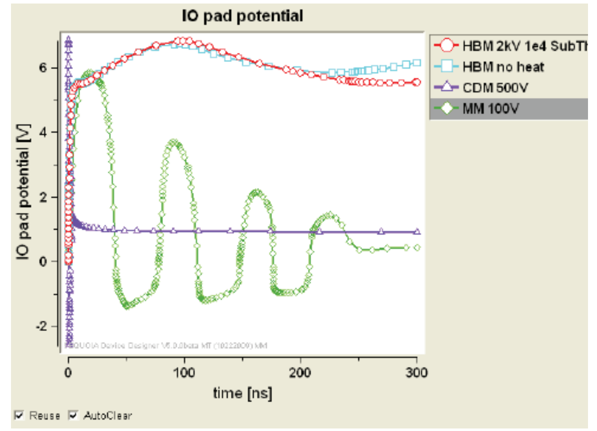

Fig. 9. Potential of the I/O pad versus time during HBM, MM and CDM ESD events.

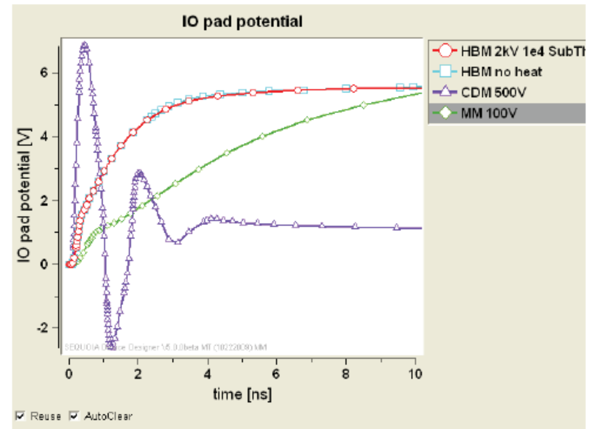

Fig. 10. First 10ns of the potential of the I/O pad versus time during HBM, MM and CDM ESD events.

a weakly damped non-sinusoidal oscillation with several periods, CDM is also oscillatory but extremely fast as shown by the first 10 ns of the pad potential waveform in Fig. 10.

In this circuit, protection from positive voltage stress at the I/O pad is provided by the current routed via diode D0 toward the protection device M2, a snapback device which shunts it to ground. On the other hand, protection from negative stress (negative half-waves) is achieved by diode D1 simply connecting the pad node to ground. This difference is very clear in the asymmetric behavior of the pad potential during MM stress. The negative half-waves have smaller peaks only slightly exceeding the diode built-in voltage of ~1V. The positive half-waves are limited by MOSFET M2 turning on and interconnect, their peak values are determined by properties of M2 and interconnect leading to it.

Further information about circuit behavior is obtained by looking at various internal currents. As shown in Figs. 11 and 12, high currents flow in the output buffer NMOS M1 for all discharge types, especially for CDM an HBM. Heating is however only an issue during HBM due to its relatively long duration, although permanent damage is likely to be avoided

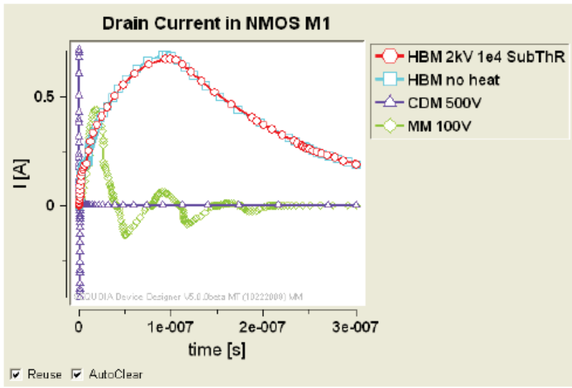

Fig. 11. Drain current in I/O buffer NMOS M1 during HBM, MM and CDM ESD events. Highest current occurs during CDM, while highest thermal stress during HBM due to its longer duration.

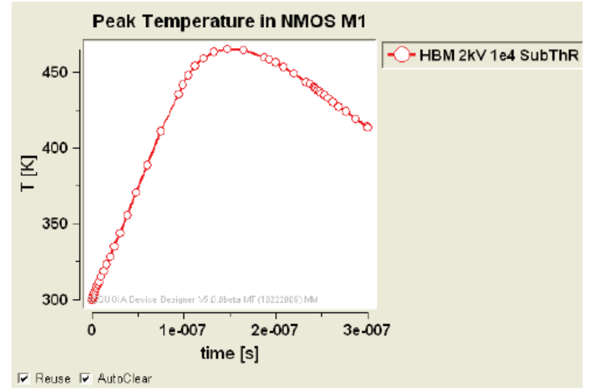

Fig. 12. Peak temperature in I/O buffer NMOS M1 during a 2kV HBM event. Significant heating is observed, although permanent damage to the device is likely avoided in this case due to its relatively large width.

in this 2kV HBM case.

The peak temperature in MOSFET M1 shown in Fig. 12 stays below 460K for all discharge types. This temperature is safely below likely damage thresholds for this device, such as aluminum melting point at ~900K or dopant redistribution at around the same or higher level. The fact that heating is only moderate despite significant current flow is due to the large width=300μm of this output driver device.

After an initial analysis of the circuit, the designer may choose to undertake additional simulations, all relatively easily done at this point. These may include:

- determine sizing and configuration of the protection circuit necessary to avoid triggering of I/O buffer devices M0,M3,M1,M4.
- determine maximum interconnect resistance R28, R29 (and thus layout distance between the I/O pad and protection device) which can be tolerated for still acceptable protection capability.
- determine the optimal configuration of the R17C1 filter controlling the gate of the protection MOSFET M2. Different RC values will cause M2 to trigger faster or slower as needed by pulling the gate up to higher potential temporarily at the start of the ESD event and thus facilitating triggering of M2.
- other issues.

V. Buck DC-DC Converter with a DMOS Switch

A. Mixed-Mode simulation of power circuits

Power devices have long been an important application area for device simulation. In comparison to VLSI devices, there is much greater variation of device types and geometries resulting in a greater need for simulation since analytical models are less likely to be accurate or even available. Matching this need, power device dimensions are in general much larger than those of VLSI devices, which means that many of the underlying physical effects are well understood and can be modeled accurately. However, the larger dimensions and richer

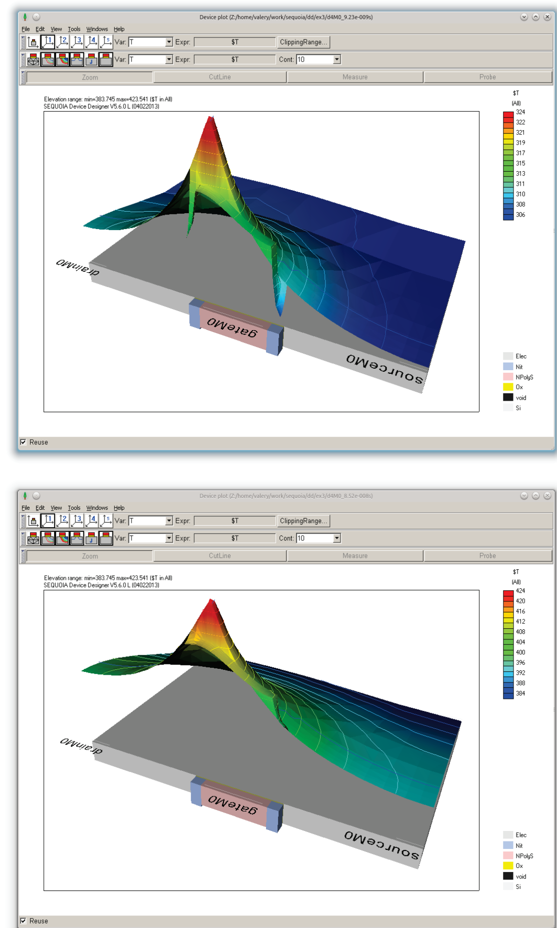

Fig. 13. Temperature distribution in I/O buffer NMOS M1 during a 2kV HBM event. Heating is shown as color (scale on right) and elevation as a surface projection plot, viewed from the gate. The top plot shows heating at 9ns from the start of the HBM event, bottom plot shows heating at 85ns near the peak heating point (see Fig. 12). Significant heat is generated in the drain junction due to the high electric field there and therefore high value of the heating term $\vec{J} \cdot \vec{E}$ in eq. (4). As more time passes the heat energy spreads away from the origin of heating and the distribution becomes less localized.

geometry of power devices makes their simulation numerically more challenging.

Device-level simulation of individual power devices can be used to extract basic electrical properties of these devices, such as for example threshold voltage, saturation current, etc. for MOSFETs and, importantly for power devices, their breakdown voltage. These electrical property metrics are then used to judge the performance of devices when used in a real-world circuit. This is however problematic in many cases due to the mutual interaction between the power device(s) and the circuit they are used in.

For example, the breakdown voltage of a power device may be highly dependent on the rise time of the external stress applied to it as well as the type of load (e.g. inductive, capacitive, etc.) attached to the device. This is due to various distributed charging effects resulting from the relatively large size of power devices and can only be handled well by transient distributed (microscopic) simulation. The actual device performance is therefore in general a function of the overall circuit and cannot be analyzed in isolation from its circuit environment. Similarly to ESD applications, this analysis is done using mixed-mode circuit-device simulation, where the device (or devices) is embedded in a sufficiently realistic circuit.

To demonstrate the importance of circuit-device interaction, Fig. 14 shows a set of transient IV curves obtained for the diode in Fig. 7 under HBM-type stress with varying values of the series inductance. For faster discharges (smaller inductance) a substantial voltage overshoot is observed due to the finite charging time of the diode. Only for the slowest cases does the IV curve approach the DC behavior of the diode, in other cases it would be difficult to predict the outcome without detailed simulation. Diode behavior becomes much more complex for MM (machine model) or CDM (charged device model) type discharges due to their oscillatory nature and high speed. Fig. 15 shows the same HBM-type transient IV curves as shown in Fig. 14 with the MM curve (red crosses) added to it. Very high voltage overshoots and oscillatory behavior are clearly visible. Note that all this complexity occurs within a very simple circuit with only one simple FEM-type device – a diode.

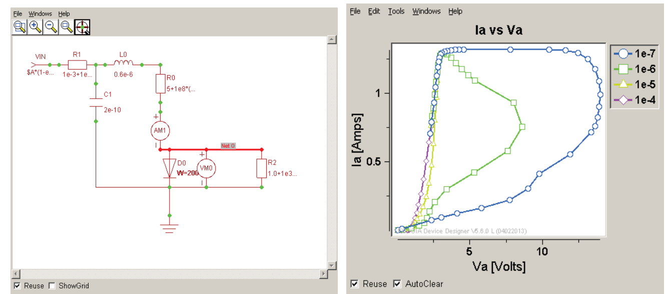

Fig. 14. Transient turn-on behavior $I_{anode} vs. V_{anode}$ of a diode for HBM-type events with varying inductive loads. The simulation circuit is shown on the left, transient IV curves on the right, the parameter is inductance value shown in the graph legend (1e-6H is HBM as in Table I). Significant charging time needed to turn on the diode leads to strong voltage overshoots for fast events, HBM or faster. The charging time is a function of process technology (doping profiles) and device geometry, such as STI width and depth, and would be difficult to predict from the DC behavior of this device. This becomes much more of an issue for more complex devices, e.g. power MOSFETs, DMOS, IGBT, SCR, so that simulation is needed to predict circuit behavior.

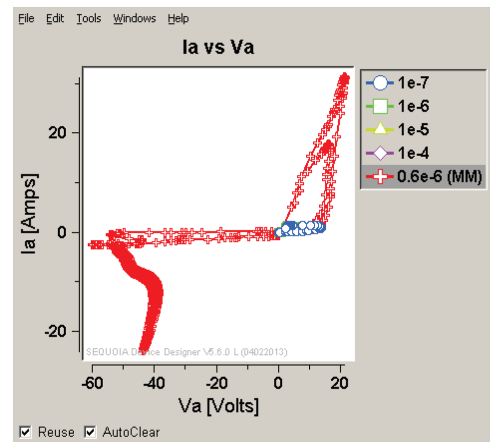

Fig. 15. Transient diode behavior as in Fig. 14 with machine model (MM) stress results added to the HBM-type stress data. Much higher overshoots due to higher injected currents are observed. Since MM events are oscillatory (see for example Fig. 9), the diode is driven into high reverse bias and breakdown is seen for $Va < 0$ on the left-hand side of the plot. It would be difficult to adequately predict the behavior of even this simple circuit from analytical diode models or even single-device analysis without the use of mixed-mode circuit-device simulation.

B. Buck Converter

DC-DC buck converters are one of the most widely used power circuits found in many millions of power supplies. Conversion efficiency, reliability and cost are therefore carefully optimized and mixed-mode circuit-device simulation is an effective design tool for this task. Here we consider a buck converter circuit with a lateral DMOS (double diffused MOS) switching device. The circuit uses 600V at input and delivers 48V at a 1A load. As shown in Fig. 16, in addition to an FEM-level models for the DMOS device and a diode, the circuit contains a driver implemented using compact transistor models (BSIM3 in this case) as well as a number of passive elements.

After the mixed-mode circuit has been defined, the next step in setting up the simulation is to create device models. The diode model used in this circuit is similar to Fig. 7. The DMOS structure and doping profiles are imported from two-dimensional process simulation previously performed by the customer with TSUPREM-4. The process simulation structure and mesh are shown in Fig. 17. The node count of this mesh is very large (∼20000 nodes) and mesh node allocation and element quality are not well suited for device simulation, poor quality (obtuse) triangles can be easily seen even at this level of magnification.

As discussed in [11], to reduce mesh size and improve its quality it is usually desirable to replace the process simulator mesh with one better suited for device simulation. An

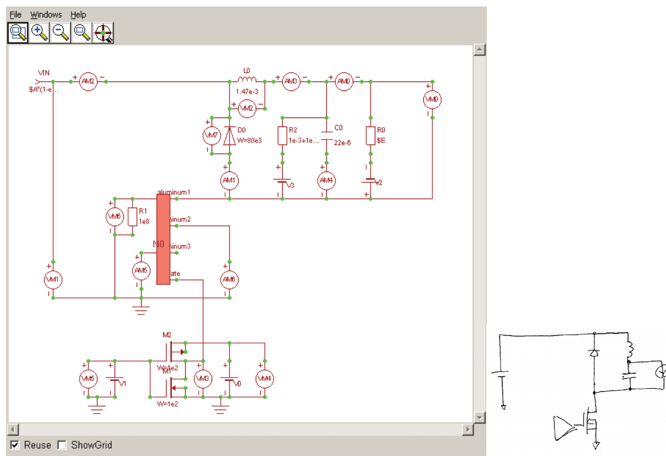

Fig. 16. DC-DC converter buck circuit with a DMOS switch. FEM models are used for the DMOS N0 and diode D0. To illustrate the circuit structure, a hand-drawn schematic is also shown on the right-hand side of this Figure. This drawing was provided to us by the engineer which requested this simulation as part of the specifications.

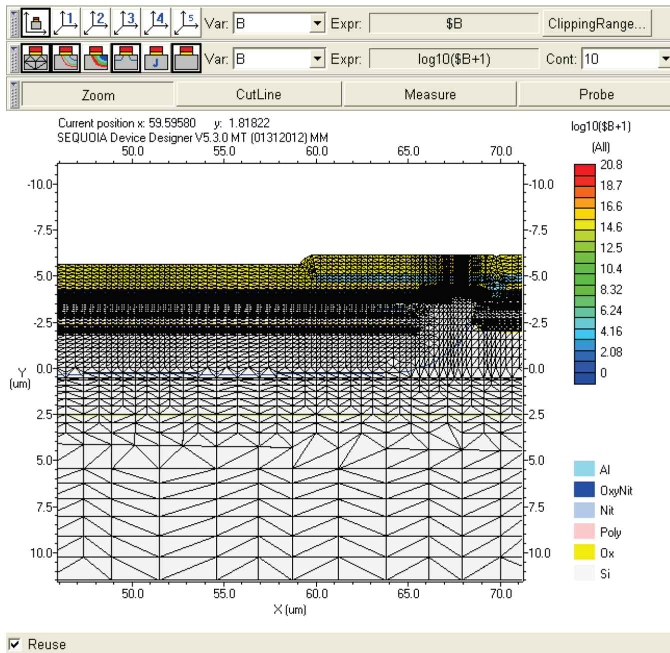

Fig. 17. DMOS mesh as generated by the two-dimensional process simulator TSUPREM-4. The mesh contains ∼20000 nodes and is not suitable for device simulation due to excessive CPU demands and related convergence issues as described for example in [11]. A large number of poorly shaped mesh elements (obtuse triangles) can be clearly seen.

optimized mesh, such as the one shown in Fig. 18, places elements of appropriate size and shape in areas important for device simulation only, typically resulting in a greatly reduced mesh node count and much improved mesh quality. Both improvements together can lead to orders of magnitude faster device simulations, in the case shown here the overall speedup is $\sim 100X$.

A particular challenge with this simulation is that the buck circuit can require many periods of the driver clock

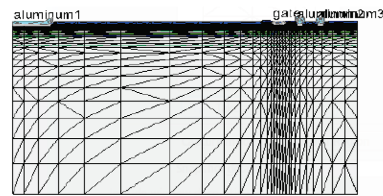

Fig. 18. New mesh created for DMOS device simulation. The node count is greatly reduced at 1217 nodes, at the same time mesh quality is improved substantially with a resulting reduction in simulation time for the buck circuit from several days to about 30 minutes or $\sim 100X$.

to reach its steady-state. Each clock cycle involves turning the DMOS switch on and off under inductive load, a non-trivial simulation which requires a substantial number of time steps with automatic time-step control for accuracy and convergence. Solving for many clock cycles may therefore require significant computational effort, for this circuit about 10 minutes simulation time is required for each clock cycle on a quad-core machine.

Results shown in Fig. 19 were obtained for six full cycles of the 100kHz clock. The DMOS switch driving an inductive load is periodically turned on and off (current labeled as "input" is also the DMOS switch current and is shown with red diamonds). Each time the DMOS turns off, the diode takes over (blue diamonds) and conducts the current flowing through the inductor (yellow triangles) Fig. 20. As indicated by the inductor equation $V = L\frac{di}{dt}$, inductor current cannot change abruptly and shows an approximately sawtooth pattern, rising when the DMOS switch is on and external energy flows into the circuit, falling when the switch is off and energy is consumed in the resistive converter load R_0.

Complex turn-on and turn-off effects can be seen in the diode and DMOS currents, such as current spikes during diode turn off due to charge storage in the diode, and current and voltage overshoot during diode turn on Fig. 21. This behavior is similar to the one shown in Fig. 15 and is a function of specific circuit timing and process technology. Both contribute to energy losses and can also lead to device stress and reliability problems and must therefore be carefully analyzed and minimized as far as possible by appropriate circuit or technology measures.

A key issue in the design of the buck converter is keeping its power loss as small as possible. Power losses occur as heating in the diode and the DMOS switch. These losses can be calculated from buck circuit simulation results as current times voltage products for both devices. Results are shown in Fig. 22 for one clock cycle. In this case the largest losses occur during the turn-on of the DMOS device, greater than 14kW for a brief period of time during turn on, when drain current is already flowing but the drain-source voltage has not dropped yet. Large losses (close to 3000W) also occur in the diode at the same time, as the diode turns off and charge, stored in the diode during its on-state, has to be removed first before current flow stops. Average losses over the entire clock cycle (root mean square average – RMS power) are ∼460W for the

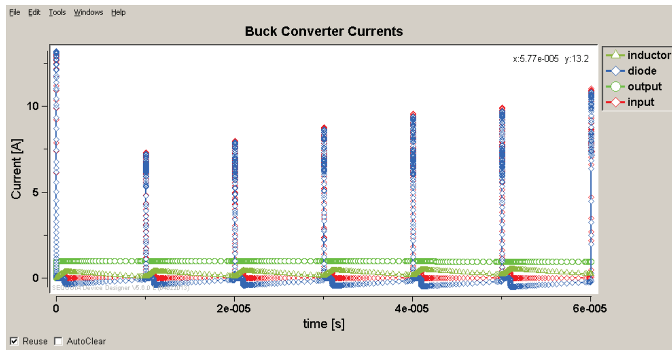

Fig. 19. Internal current waveforms for six clock cycles of the buck converter at 100kHz clock rate are shown. While the output current closely follows the set target value of 1A, the inductor current and diode current show large movements. In particular the diode is repeatedly turned on and off, showing large current spikes as the diode is turned off and is drained of the charge stored in it during its on-state.

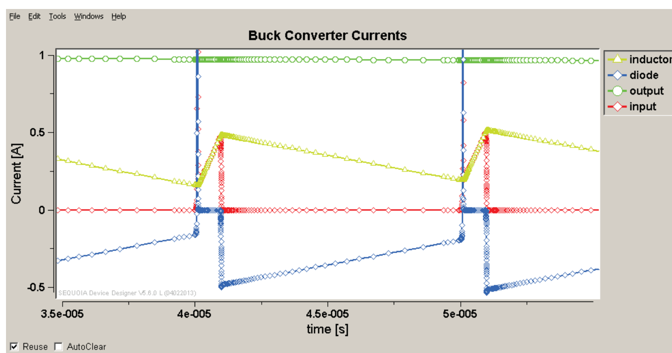

Fig. 20. Current waveforms during one clock cycle. Input current (red) flows into the inductor when the DMOS switch is open. When the switch turns off (opens) the inductor current continues to flow through the diode (blue).

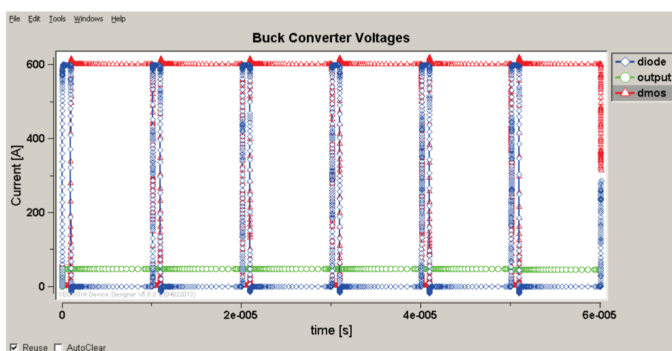

Fig. 21. Voltages across the diode and the output voltage in the buck circuit. While the output voltage is close to the target value 48V, the diode voltage rises to 600V when the DMOS switch turns on and drops close to -1V (its forward voltage with some voltage overshoot during diode turn-on) when the DMOS turns off and inductor current is re-routed through the diode.

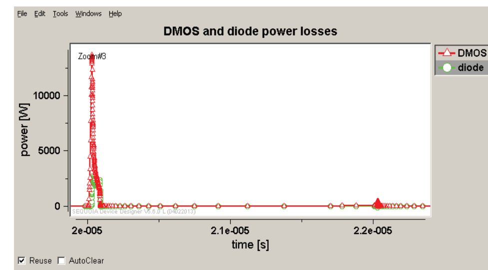

Fig. 22. Power losses in the diode and DMOS switch during turn-on (peaks on the left) and turnoff (much smaller peaks on the right) of the DMOS switch. More power is lost in the DMOS than the diode in this case. Peak power losses are high and reduce the efficiency of this buck converter. Optimization of this circuit under constraints of the utilized process technology is important to improve its efficiency.

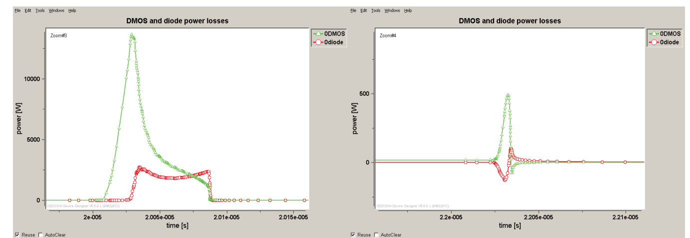

Fig. 23. Power losses versus time for the DMOS and diode during DMOS turn-on (left) and DMOS turn-off (right).

DMOS and ∼120W for the diode.

Losses during the second switching event in each clock cycle, when the DMOS switch turns off and the diode turns on, are much smaller in comparison as can be seen on the right-hand side of the plots in Fig. 23.

VI. Summary and Conclusions

Numerical simulation is an essential tool in the design of integrated circuits. It helps engineers gain understanding of circuit operation, analyze potential or real problems and design solutions. Conventional circuit simulation with SPICE-like tools and compact analytical models for circuit elements has been widely used for this purpose and enables simulation of circuits with thousands of active devices. Limits of this approach become apparent as limitations of analytical models with respect to their ability to capture physical effects. This is in particular true for ESD design, power circuit design, latchup analysis and other areas where complex physical effects or complex geometries play an important role but cannot be adequately described by compact analytical models.

Mixed-mode circuit-device simulation was introduced two decades ago to address these applications. In essence, mixed-mode adds FEM-level models to conventional SPICE-type circuit simulation, or conversely adds SPICE-type circuit equations to FEM-level equations for one or several discretized devices. The result is a circuit-level simulator with physical-level FEM models for selected devices. With such tools it is possible to study the operation of semiconductor circuits in areas not accessible to conventional SPICE, such as ESD and others mentioned above. The benefit of this approach

is improved physical accuracy, the trade-off is naturally an increase in computational cost, or an equivalent reduction of maximum possible circuit sizes.

This paper presents an overview of the mixed-mode approach, followed by two demonstration examples: one from ESD design, another one from power circuit design. Details about the steps needed to execute this type of analysis are shown, and simulation performance is discussed.

Mixed-mode circuit-device simulation is currently used as a practical design tool to address circuit issues, which cannot be handled by conventional SPICE-type tools due to limitations of their analytical device models. Mixed-mode simulation provides a physical extension of SPICE by including FEM-level models in SPICE circuits.

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