A Novel Approach to Simulate the Effect of Optical Proximity on MOSFET Parametric Yield

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Abstract

A simulation procedure to quantify the effect of process variations of mask making and photolithography on MOSFET performance and parametric yield is proposed. Dense layout of 0.16 μm six-transistor SRAM cell was used. Firstly, the accuracy of optical proximity correction (OPC) of gate layout was verified by two-step simulation of mask and photoresist pattern. This was followed by the extraction of channel length dependent MOSFET drive current for the different OPC serif and misalignment options within the corresponding process latitudes. Finally, parametric yield was simulated based on statistical distributions of MOSFET parameters.

Introduction

IC manufacturability is increasingly more dependent on the quality of photolithographic mask. Optical Proximity Correction (OPC) serifs which enhance pattern resolution on wafer for deep submicron layouts are particularly vulnerable to the quality of mask making process. Placement on line ends and in layout corners subjects the serifs to process-induced rounding. Also, the designed serif size, often much smaller than that of MOSFET channels and connecting lines, is close to mask resolution limits and therefore difficult to control. At the same time, for layouts of extreme densities, such as those in high performance SRAM cells, device tolerance for line end rounding requires highly accurate serif reproduction. The differences between the drawn and on-mask serif size and shape as well as intra-mask variation, may no longer guarantee transistor performance within specified limits. However, state of the art simulation tools assume perfect process of pattern transfer from layout to mask, with no margin for variations of OPC serif size. While the latitude of such process could impact transistor parameters, no work has been done to theoretically link its accuracy to the final yield loss due to MOSFET degradation.

In this work, we evaluated MOSFET parametric yield loss related to the process window of pattern generation. We used novel, two step procedure to simulate the shape of MOSFET gate, by first simulating the mask followed by simulating the photoresist pattern [1,2]. In the process, we subsequently calibrated the simulation to SEM images of the mask and of poly pattern on wafer. Device parameters were then extracted for serif sizes and misalignment corresponding to the mask making and photolithography process windows. We used high density, single wordline six transitor SRAM cell for 0.16 μm technology with complex OPC based mostly on hammerhead serifs. All optical simulations were done using Prolith2 software from Finle, and device/yield simulations – on Sequoia Device Designer [3].

SRAM Cell

Fig.1 shows the key layers of the single wordline 6T SRAM cell. While its area of 2.3 μm^2 should be considered as small for the set of design rules [4], the design is challenging due to the complex poly layout. It requires simultaneous optimization of FET channel CDs, contact areas (feature 3 in Fig.1), and proximity corrections: line-end-to-line (feature 1 to feature 5 in Fig.1) and line-end-to-line-end (feature 2 in Fig.1 to feature 2 of the neighboring cell).

To realize the cell, line end serifs were proposed based on an initial round of the simulation, to arrive at cell layout as shown in Fig.3. Sensitivity of the cell to OPC features, as measured by transistor performance corresponding to the variations of pattern transfer from design to wafer, was verified below.

Simulation Procedure

A. Optical Simulation.

In general, pattern transfer from design to wafer involves mask generation followed by photolithography. We adopted a corresponding two-step optical simulation scheme shown in Fig.2 [1,2]. We first simulated the reticle followed by simulating the photoresist pattern on silicon. First level input, drawn design plus OPC serifs (hammerheads) (Fig.3), was used to generate bitmap of the mask. Second level input was either the drawn design with OPC serifs (control), the extracted bitmap of the mask simulated in the first round (the actual two-step simulation), or the extracted bitmap of the real mask based on its SEM image (calibration of the simulation, Fig.4).

In the mask simulation, we used standard illumination with drawn feature sizes blown up by 4x, to provide the desired effect of mask corner rounding. Bitmaps for the second step of the simulation were obtained from the aerial image of the intensity contour corresponding to the target FET CD (here, 28% intensity).

A comparison of Figs. 3 and 4 shows line end rounding of hammerheads due to the mask writing process. Fig.5 shows contour overlays: simulated mask, drawn data and SEM image. Fig.6, a detailed view of the gate line end, shows that mask corner rounding was simulated with the accuracy of about 5 nm, compared to the much worse accuracy of drawn layout to mask overlay of about 20 nm.

To simulate or print photoresist on wafer, we used annular illumination (NA=0.6, 0.75/0.45 outer/inner diameter). The simulated intensity contour of ~30%, called the CD contour, corresponded to the channel length (CD). At the same time, the effects due to the exposure defocus and photoresist

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scumming were modeled by the intensity contour of 10% higher than that of the CD contour, referred to as the Process Corner (PC) contour.

The entire process of optical simulation: from mask to pattern on wafer, was calibrated based on SEM images of the photoresist (Fig.7). Fig.8 and 9 show the overlay of the final pattern and intensity contours simulated from: a) drawn layout, b) simulated mask, c) SEM of the mask. The best agreement was achieved for the simulated mask pattern.

B. Electrical Simulation.

Having calibrated optical simulation from design to gate pattern on wafer, we then simulated the effect of mask variation and misalignment on optical proximity and the resulting degradation of transistor performance and parametric yield [5]. As first step, we looked into the effect of serif size variation within mask CD tolerance, at mean to target difference of 10 nm (1x). Fig.10 shows a detailed view of simulated mask corresponding to such serif variations, and the corresponding CD and PC intensity contours. The photolithography magnifies the barely visible difference of serif size and creates channel length distribution along its width. This, combined with gate misalignment, affects MOSFET drive and leakage currents. Fig.11 shows examples of gate/diffusion overlay, for the different serif size and misalignment options. One can expect that, compared to the nominal serif (center, Fig.11b), too large serifs (11a) increase the margin of misalignment, but reduce drive current, whereas too small serifs (11c) make the transistor susceptible to short channel effects.

To estimate the impact of corner rounding, CD variations, and misalignment on transistor performance and yield, the width of simulated poly gates was measured at a number of locations. The channel was divided into small sections across its width and statistical distribution of MOSFET gate length was extracted. It was necessary to assume that the gate length varies slowly across the MOSFET width in comparison to the line width itself. This is a valid assumption since the relevant curvature radius can not be smaller than the stepper wavelength. As a result, each transistor in the cell was viewed as a number of connected narrow transistors (slices) of varying gate lengths. Here, we divided the channel into 16 sections, each one 20 nm long. A more accurate but practically not feasible approach would require solving Poisson's and continuity equations in three dimensions over the entire channel region. However, our approximation was sufficient for yield evaluation to sort out the "passing" and "not passing" devices.

C. Yield simulation.

The above assumption enabled us to carry out statistical analysis of transistor performance and yield. We estimated the properties of cell transistors by the statistical distribution of poly line widths. Fig.12a shows channel length dependence on the position along y-axis in Fig.11, for the different misalignment options.

Depending on the technology, a transistor may be more or less sensitive to gate length variation. For this work, we used a simulated drain saturation current I_{DSat} vs. channel length L_{poly} dependence shown in Fig.12b. For each misalignment condition, yield estimates were generated based on channel length and drive current histogram shown in Fig.13. These histograms were then mapped into I_{DSat} histograms (Fig.14) using the I_{DSat} vs. L_{poly} curve from Fig.12b. Yields were estimated for each misalignment option by calculating a percentage of samples with low I_{Dsat} or high leakage. Fig. 15 shows that final yield loss can range up to 30%.

Die-to-die and wafer-to-wafer variability and the corresponding yield losses can be considered by generating gate length curves as shown in Fig.12a for the expected lithography and etch variations. This would affect the calculated gate length and I_{DSat} histograms, and would be reflected in the yield loss.

Discussion

Based on the assumed process margins for photomask generation and photolithography, we evaluated parametric yield of a high density SRAM cell. The yield loss on the order of 30% was the result of serif size variation combined with misalignment. This result demonstrates the capability of the procedure to establish requirements regarding placement of MOSFET gates, endcap length and proximity to other poly lines. As a broader goal, the simulation would help determine the tradeoff between the cell size and the toolset used in the manufacturing. In the case of unacceptable yield loss emerging from the simulation, the cell would have to be redesigned, or better stepper and reticle grade would have to be used.

Conclusions

In summary, in this work we demonstrated for the first time a consistent simulation path from drawn layout to yield on wafer. The procedure consisted of subsequent simulations of the photomask, photoresist pattern on wafer, extraction of MOSFET channel length distributions, simulation of MOSFET parameters (drive or leakage current), and finally simulation of parametric yield. The integrated approach of yield simulation should be an important element of design verification.

References

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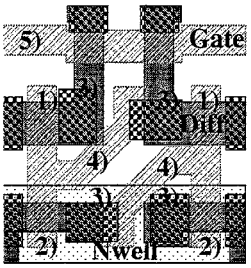

Fig.1. Key layers of SRAM cell. Critical areas: endcaps (1,2), contact areas (3) 45 deg arm (4), wordline (5).

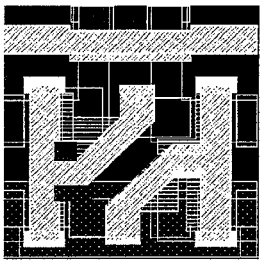

Fig 3. Poly gate layer with serifs added by CAD flow.

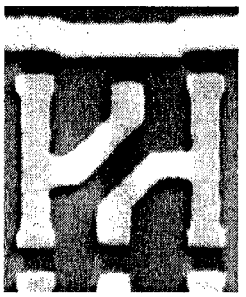

Fig 4. Gate mask: SEM picture.

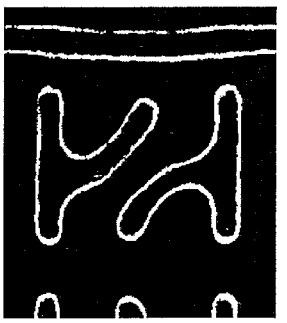

Fig 7. Gate pattern on wafer: SEM picture.

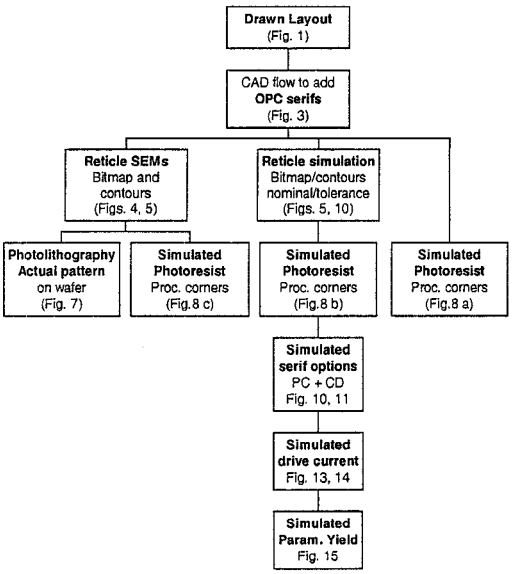

Fig.2. Simulation scheme adopted in this work.

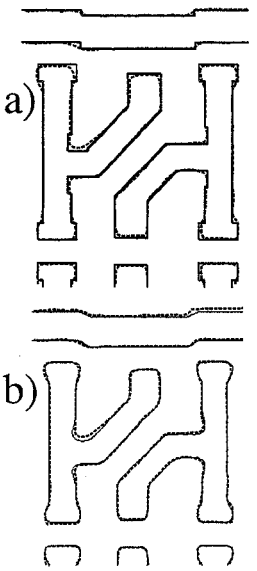

Fig 5. Gate mask: SEM contour overlaid with drawn layout (a), simulated mask (b).

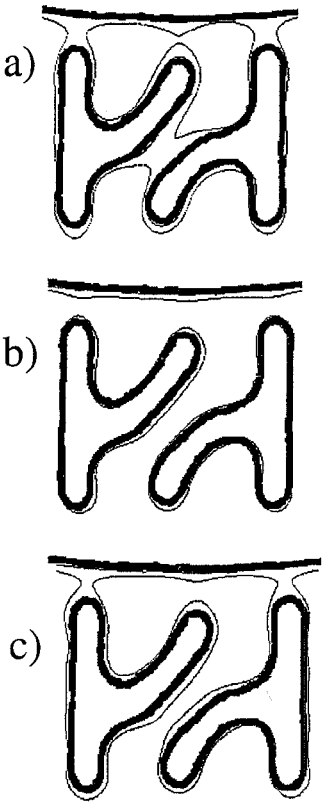

Fig 8. Gate pattern on wafer: SEM contour (thick line) overlaid with process corner contours simulated from: a) drawn layout, b) simulated mask c) SEM bitmap of the mask. Best accuracy is achieved for b).

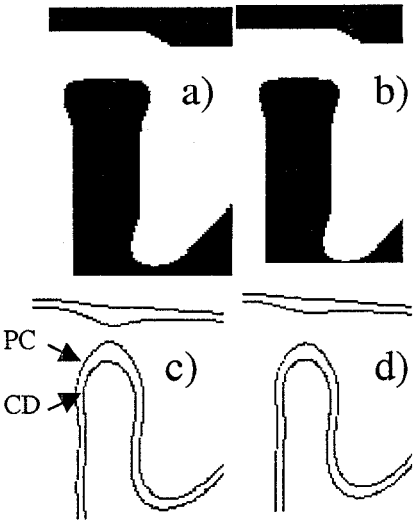

Fig.10. a, b) Detail of simulated gate mask with two serif sizes within mask tolerance (10 nm) (a-larger, b-smaller), c, d) Corresponding aerial images of gate process corner PC (outside) and critical dimension CD (inside) intensity contours.

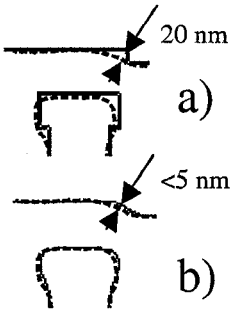

Fig 6. Verification of the simulation of gate mask: detail of SEM contour (dashed line) overlaid with drawn layout (a) and simulated mask (b), showing significant improvement in overlay accuracy.

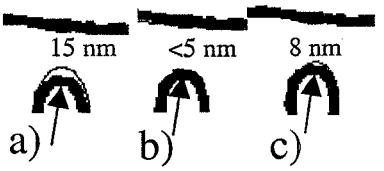

Fig 9. Verification of the accuracy of gate pattern simulation: detail of the SEM contour (thick line) overlaid with CD contours simulated from: a) drawn layout, b) simulated mask, c) SEM of the mask. Best accuracy is achieved for (b).

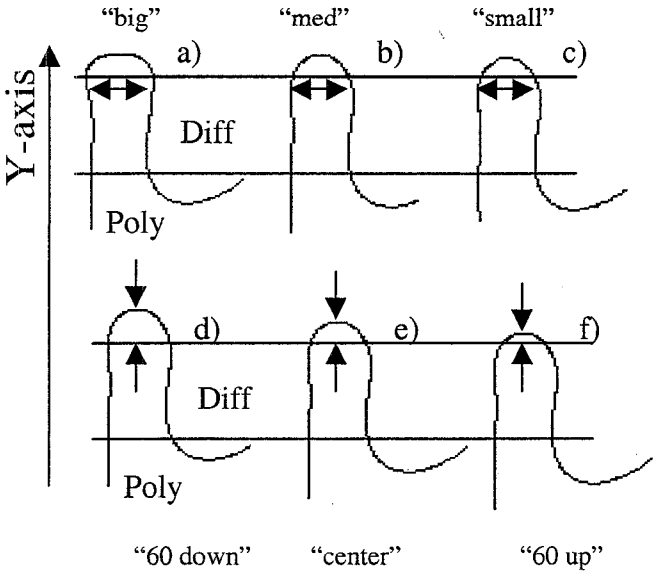

Fig.11. The effect of gate shape and alignment on MOSFET L distribution, based on simulated CD contours corresponding to: a,b,c - differences due to serif size variation, c,d,e - differences due to misalignment. Assumed shape distortion (big (a) or small (c)) along with assumed worst case misalignment of 60 nm up and down from center point (e) will be used in the subsequent yield calculations.

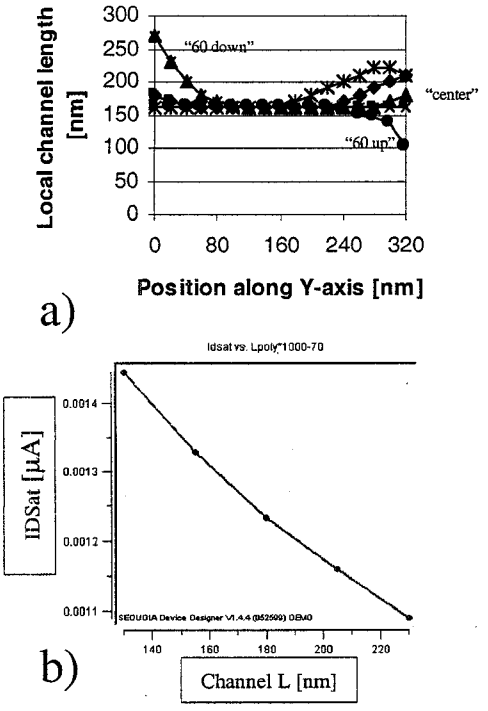

Fig.12. a) Summary of L distribution along the Y-axis from Fig.11 for the different serif sizes and misalignments, b) Calibration curve for drive current vs. channel length.

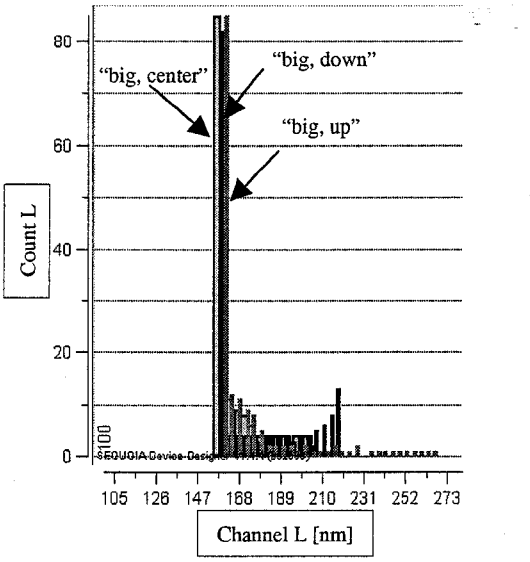

Fig.13. Example of an input for drive current simulation: histograms of channel length for different misalignment options from Fig.11.

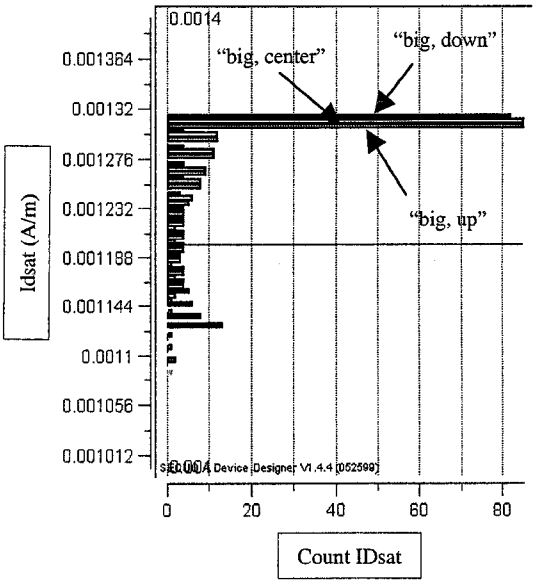

Fig.14. Histogram of drive current distribution based on data from Fig.13 and calibration curve (Fig.12 b).

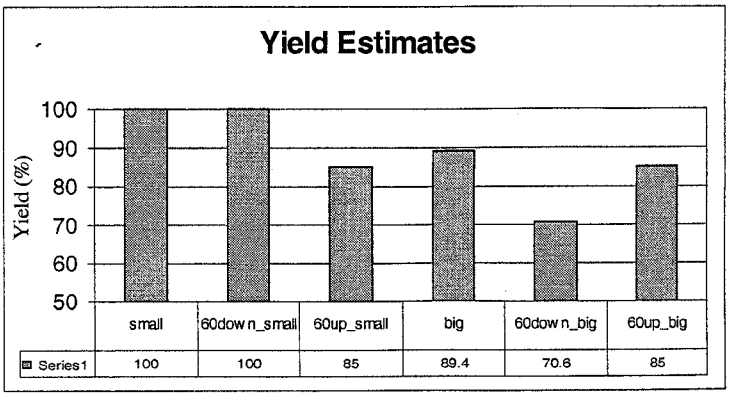

Fig.15. Yield calculation assuming different misalignment options form Fig.11, based on drive current reduction of 10% or leakage increase beyond 1 nA/um.