ESD Protection Design Using a Mixed-Mode Simulation for Advanced Devices

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Abstract - In this paper, we propose a new ESD protection design methodology using a mixed-mode ESD simulation that takes account of a coupling effect for both device and circuit. As a result, we can analysis the each protection unit operation and select the optimized protection circuits in prevention of ESD failure on separated power supply units by prediction of the simulation.

I. Introduction

Electrostatic Discharge (ESD) is one of serious problems for modern integrated circuit (IC). Thinner gate oxides, complex chips with multiple power supplies, mixed-signal blocks and faster circuit operation all contribute to increased ESD-sensitivity of advanced semiconductor products [1,2].

The ESD leads to damage to IC parts due to large energy dissipation in an extremely short time of less than 150 ns. Common ESD failures are caused by either thermal breakdown in silicon and/or metal interconnects due to high current or dielectric breakdown in gate oxide due to high voltage overstress. Therefore, a mixed-mode approach between device and circuit modeling is useful in ESD protection circuit design, since these ESD failures depend on all of impurity profile, device shape and circuit network.

In this paper, we propose a new ESD protection design methodology in system LSI using a mixed-mode ESD simulation tool in Sequoia design systems incorporation [3] that takes account of a coupling effect for both device and circuit. As a result, we have succeeded in prevention of ESD failure on signal line across separated power supply units by prediction of the simulation.

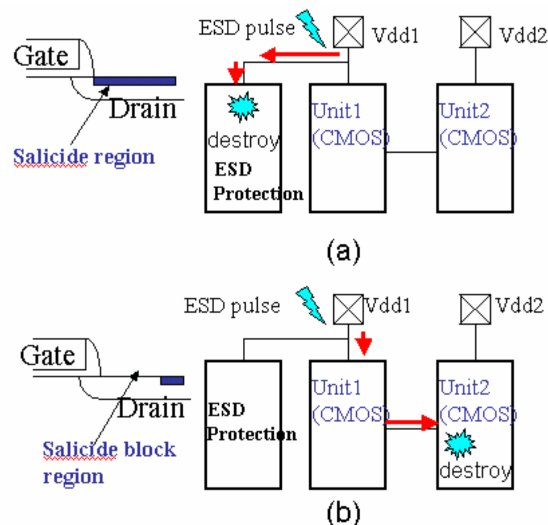


Figure 1: Schematic diagram for ESD failure on signal line across separated power supply units including ESD protection devices (a) without salicide block region and (b) with salicide block region.

II. Target Circuit

A. ESD failure on signal line across separated power supply units

Schematic explanation of ESD failure on signal line across separated power supply units is shown in Figure 1.

Self-aligned silicide (Salicide) process where low resistance region is formed on the source/drain (SD) diffusion region to lower the gate resistance (and RC delay), to reduce the SD parasitic resistance and increase the drive current of MOSFET is widely adopted in advanced system LSI [4]. ESD protection devices with the salicide region are extremely weak to ESD stress, and result in destruction.

To overcome this situation, salicide block region where the salicide is not formed on a limited part of SD region is widely used as standard approach. Although the ESD protection device with salicide block region itself becomes strong to ESD stress, ESD failure on signal line across separated power supply units is caused by faster operation in the internal circuit constituted by devices without salicide block region. Therefore, the optimization of ESD protection devices, internal devices and their circuit network is required for ESD protection design in system LSI.

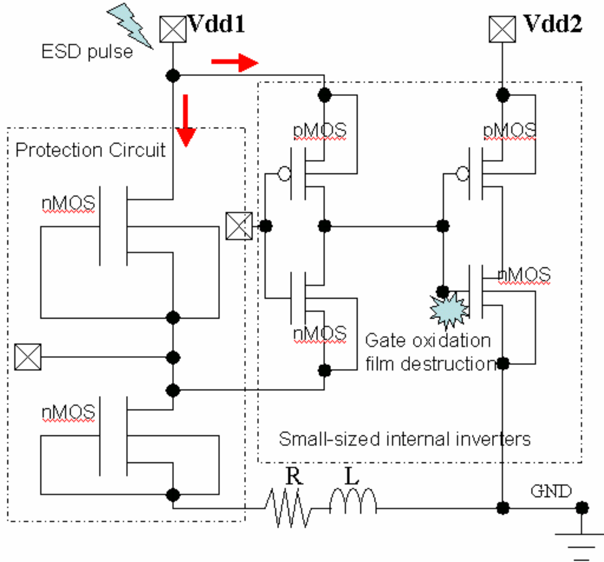


Figure 2: Target circuit diagram to investigate failure on signal line across separated power supply units.

B. Circuit under study

Figure 2 shows a target circuit diagram to investigate ESD failure on signal line across separated power supply units under our study. Although the most of total current generated by ESD stress flows in the protection circuit with MOSFETs of large channel width, the some current flows in an internal circuit. The voltage of output signal between pMOS and nMOS in the internal inverter of the first stage increases by the current which flows in the internal circuit. Therefore, it leads to increase the gate voltage

in CMOS inverter of the second stage, and its increase in gate voltage causes the destruction of gate oxidation film.

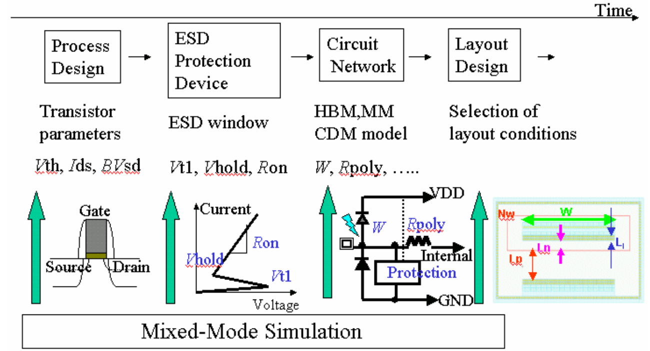


Figure 3: Conceptual figure for ESD protection design using mixed-mode simulation.

We also observed the damage of gate oxide in the measurement, but not shown here. Therefore, we investigate the increase in the gate voltage using mixed-mode simulation.

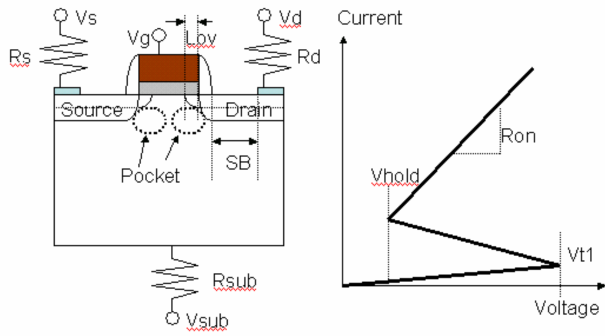
III. Simulation Methodology

Figure 3 shows the conceptual figure for ESD protection design using a mixed-mode simulation. In a process design, we make a calibrated model which reproduces basic electrical characteristics after setting up the transistor parameters which fill target. In ESD protection device design, the calibrated model is updated using the TLP measurement parameter within an ESD design window. In circuit network design, Selection of an ESD protection system and optimization of a circuit network are performed based on the prediction of mixed-mode simulation using the calibrated model for both protection and internal devices. A layout design reflects the result of the simulation.

We investigate the gate voltage of MOSFET which has caused the destruction of gate oxidation film using mixed-mode simulation. To ensure the simulation accuracy, model parameters of mixed-mode simulation are calibrated by the procedure shown in Figure 4.

The depth profile at channel center is first extracted from subthreshold characteristics with substrate bias dependence of a long channel MOSFET. The lateral profile at gate edge including the pocket profile, SD profile and the gate-drain overlap (L_{ov}) is determined from gate length dependence of their characteristics [5]. Then, parameters of carrier mobility are extracted from Id-Vg and Id-Vd characteristics. The extracted

2D impurity profile of ESD protection device is shown in Figure 5.



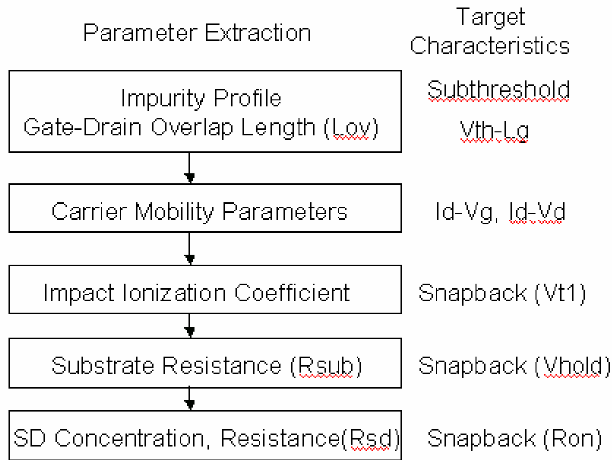


Figure 4 Model parameter calibration flow for mixed-mode simulation.

Figure 6 shows the dependence on parameters for snapback characteristics. The parameter with large sensitivity to breakdown voltage (V_{t1}) except for the pocket implantation is the impact ionization coefficient (*ii*). The holding voltage (V_{hold}) after the snapback has a large sensitivity for the substrate resistance (R_{sub}). The slope of snapback characteristics (R_{on}) depends on S/D concentration for impurity and S/D resistance (R_{sd}) largely. The S/D concentration relates to activation concentration. Therefore, *ii*, R_{sub} and *R*sd are used to adjust the V_{t1}, V_{hold} and R_{on}, respectively.

As a result, the calibration strategy of these parameters for electrical characteristics is clarified.

After the calibration of model parameters, we proceed to mixed-mode ESD simulation at device and circuit level. The calibrated physical parameters such as the impact ionization and carrier mobility models for nMOS and pMOS are common in various devices with different dimension. We assume that small size devices with fully salicide in the internal circuit have extremely small R_{on} after breakdown voltage, and deal with R_{sd} of their devices as 0Ω.

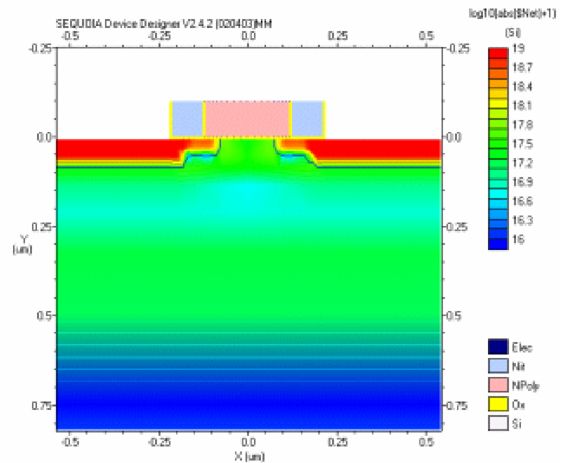
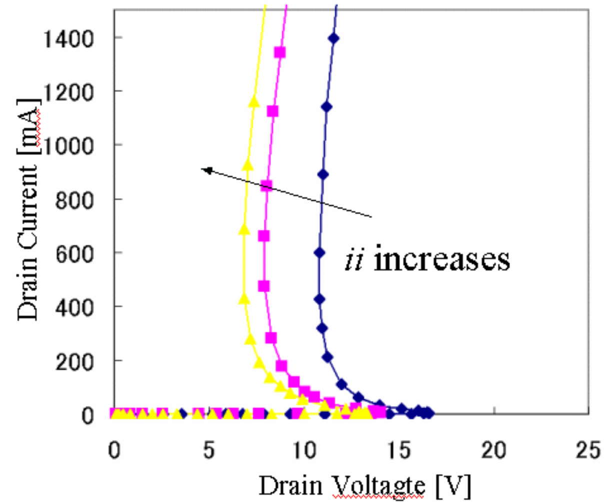
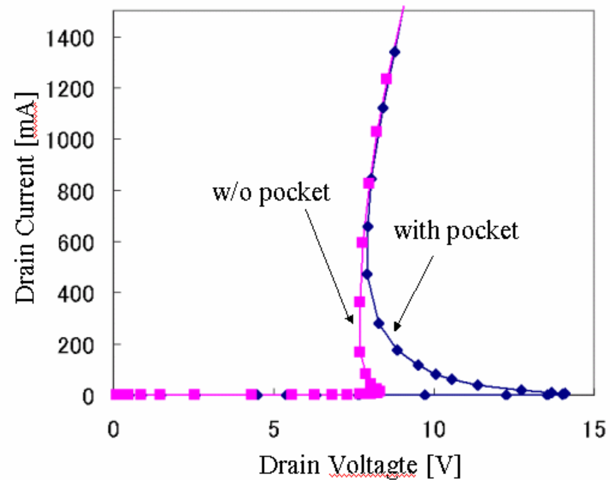


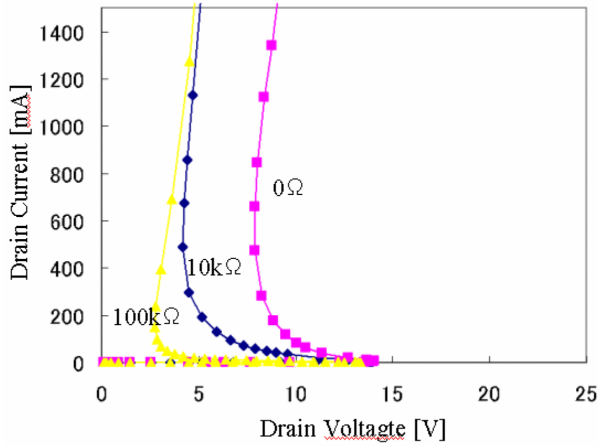
Figure 5: 2D impurity profile of ESD protection device.



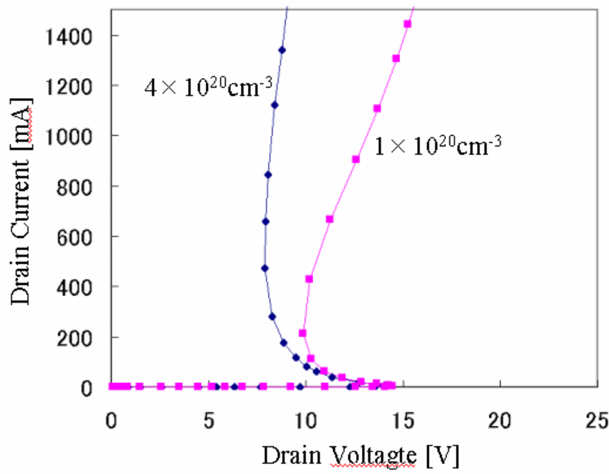
(a) *ii*



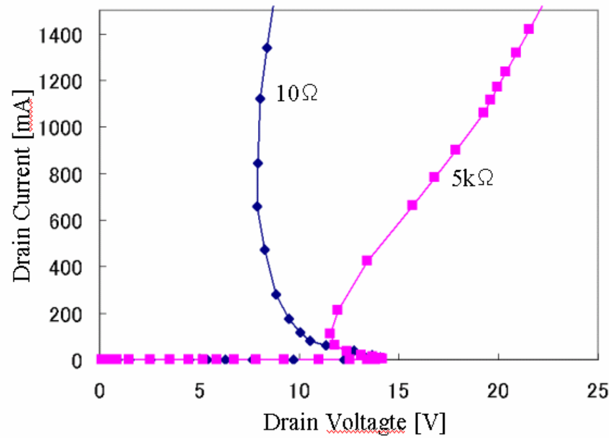
(b) Pocket implantation



(c) *R*sub



(d) S/D concentration



(e) *R*sd

Figure 6: Dependence on parameters for snapback.

IV. Simulation Result

A. Comparison to TLP measurement

The simulation with calibrated parameter in the ESD protection device with gate length of 0.49μm is compared to the transmission line pulsing (TLP) measurement. TLP measurement provides insight into ESD failure threshold and instantaneous I-V characteristics [6].

Figure 7 shows snapback characteristics of nMOS and pMOS with different salicide block length (*SB*), respectively. The common parameter set is *R*sd=3KΩ·μm, *R*sub=8KΩ·μm and the value which tuned up some default values of an impact ionization coefficient. Simulations are in good agreement with experiments for both nMOS and pMOS with *SB*=0.5μm and 2μm.

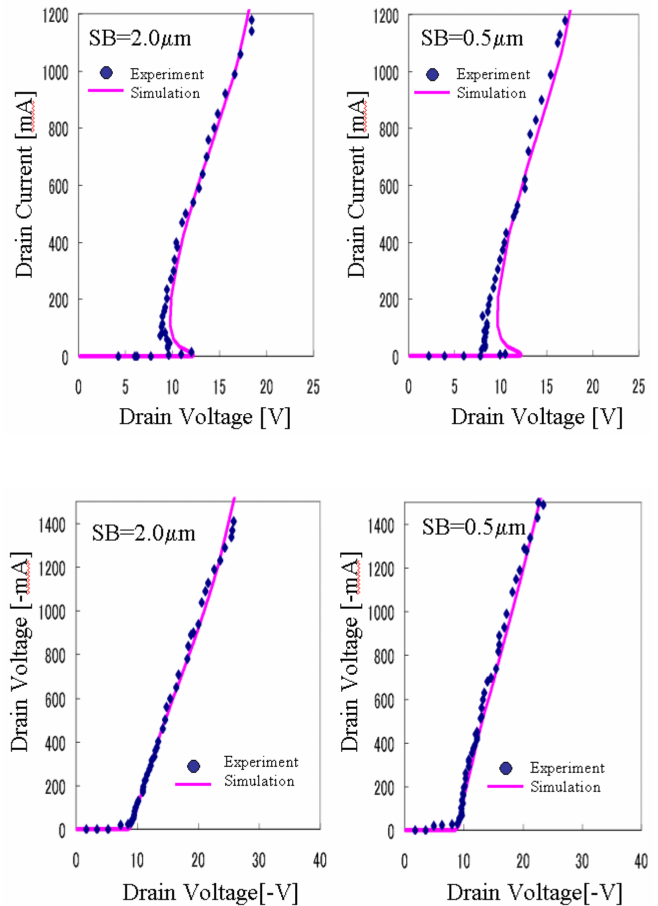


Figure 7: Comparison between experiment and simulation for TLP characteristics.

We also have confirmed that simulated basic electrical characteristics of small devices with gate length of 0.24μm in the internal circuit reproduce those of experiments.

B. ESD Stress and HMB model

In order to predict ESD operation, an actual ESD waveform must be reproduced in a simulation. In general, ESD testing models include human body model (HBM), machine model (MM), charged device model (CDM), and so forth. The widely accepted HBM model simulates ESD events occurring as a charged human body contacts an electronic part directly, with its equivalent circuit shown in Figure 8.

Figure 9 shows the simulated HBM waveform. Simulation satisfies HBM waveform requirement that pulse decay time (t_d) when the current is 36.8% of the peak value becomes 150ns ± 20ns. The more accurate prediction of ESD operation is possible by using the mixed-mode simulation which reflects actual ESD waveform, device physics and circuit network.

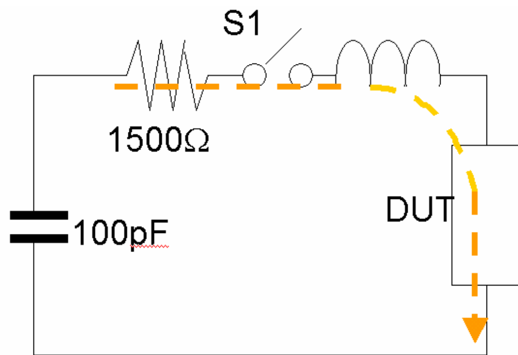


Figure 8. Simplified HBM ESD model circuit.

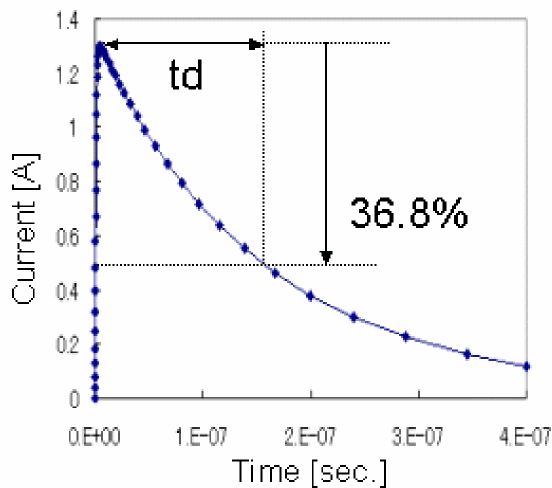


Figure 9. Simulated HBM ESD waveform.

C. ESD Protection Device and Circuit Design in System LSI

We investigate the damage in the gate oxide of CMOS inverter on signal line across separated power supply units for HBM ESD stress.

Figure 10 shows simulated gate voltage of CMOS inverter on signal line across separated power supply units in Figure 2. The peak values of gate voltage for HBM stress 500V, 1000V and 1500V are 8V, 15V and 24V, respectively. Although the voltage of output signal between pMOS and nMOS in the internal inverter of the first stage increases by the current which flows in the internal circuit, the reason why its voltage becomes larger than the breakdown voltage of nMOS in the first stage (10.5V) is not clear.

Figure 11 shows simulated source voltage of nMOS in the first stage. It is found that the source voltage increases as HBM stress bias becomes large, and the voltage between the source and the drain in nMOS is equal to the breakdown voltage in the case of 1500V HBM stress approximately. The increase in source voltage is due to parasitic resistance and inductor between the source and the ground. Therefore, it is important to optimize the parasitic resistance and inductor.

To prevent increase in the gate voltage in CMOS inverter of the second stage, we investigate the influence of inserting gate protection resistance (R_{poly}) and transistor on the gate voltage as shown in Figure 12.

Figure 13 shows simulated gate voltage of CMOS inverter on the second stage with various values of R_{poly} for HBM stress 1500V. The peak value of gate voltage is constant with 24V in all cases, and does not depend on R_{poly}. It is because the voltage drop across R_{poly} is small, since the current flows into nMOS in the first stage after instantaneous current which flows into R_{poly}.

Simulated gate voltage of CMOS inverter on the second stage with gate protection transistor for various HBM stress is shown in Figure 14. The gate voltage is suppressed at 10.5V in all cases. It is because the instantaneous current flows into the gate protection transistor as well as the case of inserting R_{poly}, and then the gate voltage is held at breakdown voltage. If the destruction voltage in the gate oxidization film is 12V, gate oxidization film destruction in case without gate protection transistor occurs at about HBM 600V.

Next, we investigate the optimization of the dimension of the gate protection transistor. Dependence on the channel width (*W*) in the gate protection transistor of the gate voltage of nMOS in the second stage is shown in Figure 15. The gate voltage for *W*<5μm becomes more than the breakdown voltage of the gate protection transistor. For *W*>5μm, the current flows into gate protection transistor instantaneously, and then the current flows into nMOS in the first stage. In contrast, for *W*<5μm, the current flows into the gate protection transistor before and after the breakdown voltage continuously, and it leads to the increase in the gate voltage by the current proportional to R_{on} after the breakdown voltage. We guess that the destruction in device is caused by the decrease in channel width of the gate protection device.

We have succeeded in prevention of ESD failure on signal line across separated power supply units by the optimization of ESD protection device and circuit which is based on prediction of the simulation.

The calculation time under the target circuit including 6 devices is about one hour using a PC of CPU performance with 2GHz. Calibration is easy because of a few physical parameters and a clear relation between parameters and electrical characteristics. Thus, the optimization of ESD protection circuit and device in a short period is possible using mixed-mode simulation.

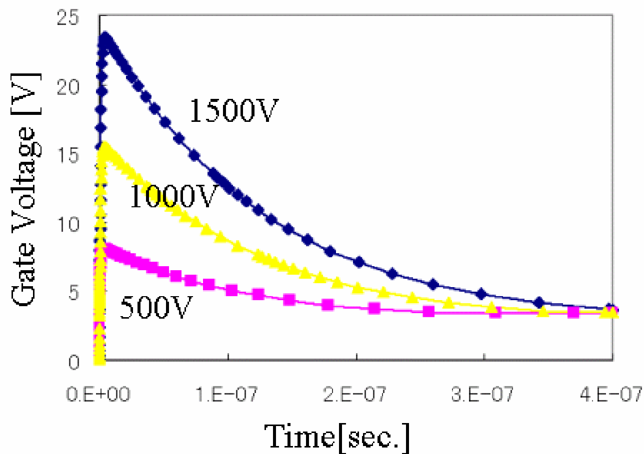


Figure 10. Simulated gate voltage of internal nMOS on signal line across separated power supply units.

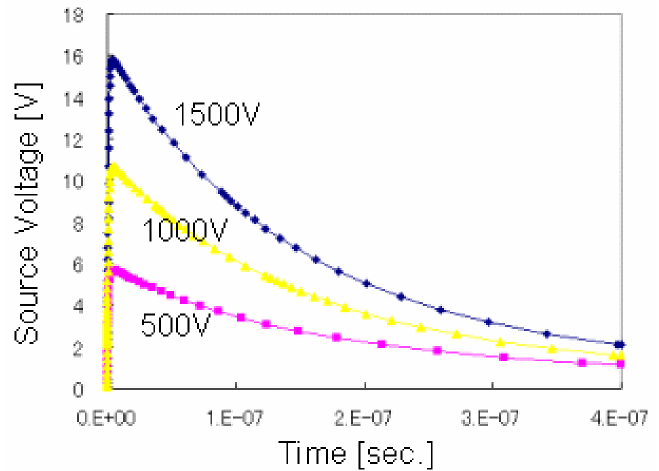


Figure 11. Simulated source voltage of internal nMOS in the first stage.

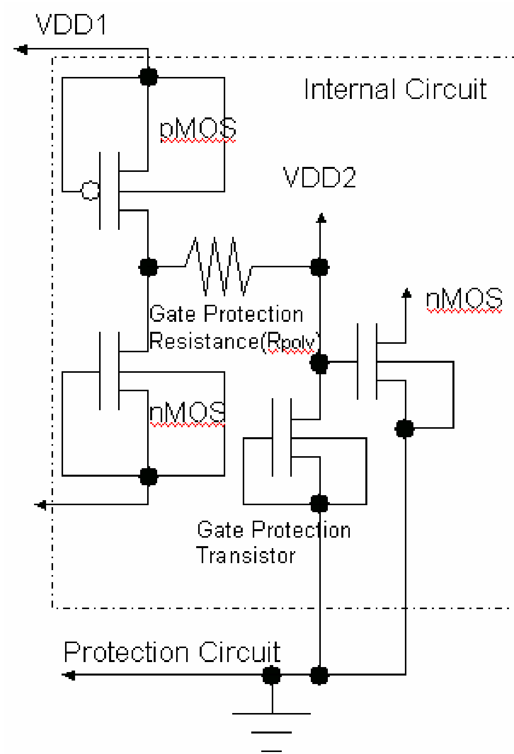


Figure 12. Target circuit diagram with gate protection resistance and transistor.

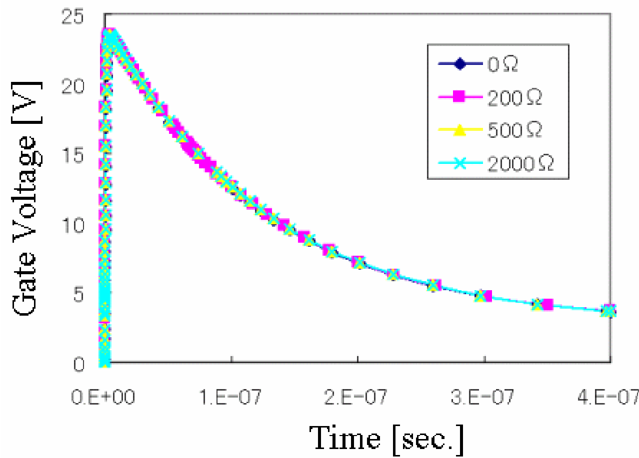


Figure 13. Simulated gate voltage of CMOS inverter on the second stage with various values of *R*poly for HBM stress 1500V.

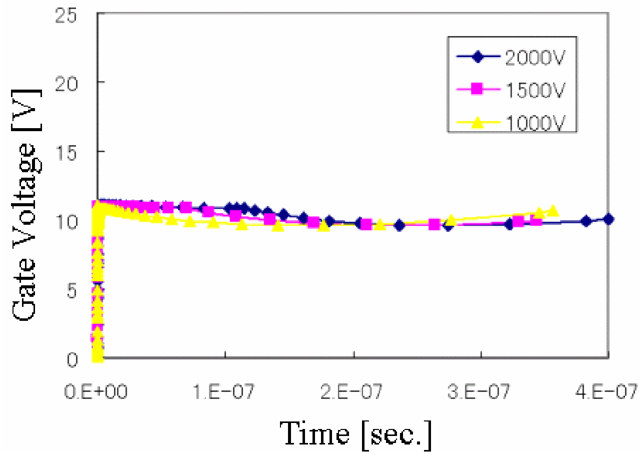


Figure 14. Simulated gate voltage of CMOS inverter on the second stage with gate protection transistor for various HBM stress.

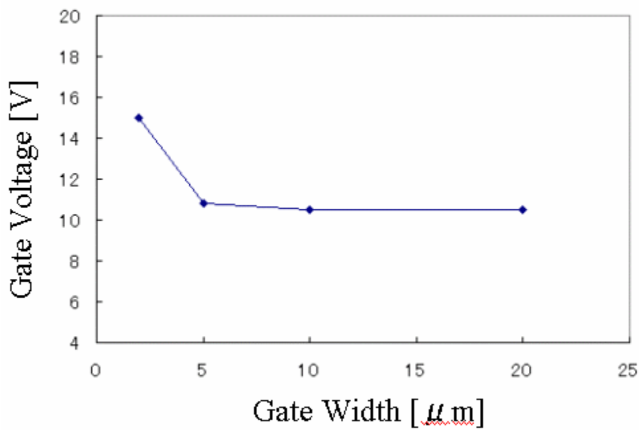


Figure 15. Dependence on the channel width (*W*) in the gate protection transistor of the gate voltage of nMOS in the second stage.

V. Conclusions

We have proposed a new ESD protection design methodology in system LSI using a mixed-mode ESD simulation. As a result, we have succeeded in prevention of ESD failure on signal line across separated power supply units by the optimization of device and circuit which is based on prediction of the simulation. Calibration is easy because of a few physical parameters and a clear relation between parameters and electrical characteristics, and our approach is effective for design of advanced ESD protection device and circuit in system LSI where a quick turn around time (TAT) is required thoroughly.

References

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