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Mixed-Mode Circuit-Device simulation of ESD Protection Circuits with Feedback Triggering

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Abstract

Accurate simulation of ESD protection devices requires physical simulation models capable of capturing all relevant physical effects. Conventional SPICE simulation does not include impact ionization, rendering this type of simulation unusable for the analysis of high-current high-voltage ESD discharge events. We analyze a modern ESD protection circuit with feedback triggering using physical mixed-mode circuit-device simulation, utilizing Finite Element Models (FEM) for MOSETs. In comparison to SPICE-equivalent simulation, qualitatively different results are obtained. Physical simulation is shown to be necessary for accurate analysis of ESD protection circuits.

Introduction

Advanced triggering circuits controlling the behavior of protection devices are an increasingly popular component of on-chip ESD protection [1], [2]. Such circuits are employed to drive gates of protection MOSFETs to facilitate triggering.

However, successful deployment of such triggering circuits requires careful optimization. Circuit simulation is an essential component in the optimization of these triggering circuits. While it is known that conventional SPICE circuit simulation cannot handle snapback-based ESD protection circuits, SPICE simulation has been reported to have been used to analyze trigger circuit-driven ESD schemes [1]. The reasoning behind it is that although SPICE cannot account for impact ionization and therefore snapback phenomena, since triggering circuits rely on gate control rather than avalanche breakdown and snapback for their operation, SPICE should be applicable.

In this paper we consider a 90nm technology feedback triggering circuit [1] shown in Fig. 1. We demonstrate that the triggering circuit does in fact depend on parasitic bipolar action for its successful operation. If impact ionization is not included in the analysis (as would be the case with a SPICE simulation), current flow through the protection device may be greatly underestimated, leading to possible rejection of a valid circuit alternative. Unphysical simulation results may lead to costly design mistakes.

Feedback Triggering Circuit Analysis

Circuit Schematic and Intended Operation

The analyzed circuit is shown in Fig. 1. The circuit includes a large protection MOSFET M3, an RC filter R4, C2, inverter M0/M4 and a latch circuit M1, M2, M5, M6. Human Body Model (HBM) ESD discharge is modeled by an RLC circuit C1, L0, R2, with the 100pF capacitor C1 pre-charged to 2000V, then discharged into the protection circuit via the 7.5e-6H inductor L0 and 1.5kOhm resistor R2.

During an ESD pulse, the potential of node RC is raised to Vdd for about 25ns (its RC time constant). During this time, inverter output inv_out is forced low, which causes the latch to turn on and keep the gate of M3 tied to Vdd. The latch stays on longer than the RC time constant, which provides sufficient time to consume the ESD pulse energy [1].

Physical-Level Mixed-Mode (FEM-Circuit) Analysis

We carry out a mixed-mode circuit-device analysis of the triggering circuit in Fig. 1. All MOSFETs are analyzed as FEM models (Fig. 2). Physical effects such as impact ionization, thermal and avalanche generation, leakage, etc. are taken into consideration. Finite Element Models (Fig. 2) for this analysis were generated using SEQUOIA device synthesis software [3]. Results are summarized in Fig. 3. As expected, RC node (Fig. 1) potential is raised by the ESD pulse due to capacitive coupling C2 between Vdd and RC. C2 is then discharged through R4 with the RC time constant of 25ns (blue curve in Fig. 3). While RC is high, inverter output inv_out remains low (red) and the latch is on. The latch keeps M3g (gate of the large protection device) high (cyan curve). When the latch turns off at 60ns, M3g drops to zero and behavior of the protection device M3 approaches the red curves in Fig. 2, i.e. grounded-gate MOSFET operation. Due to the loss of added channel conduction, the voltage drop on M3 increases (green curve in Fig. 3). However, parasitic bipolar current flow continues keeping the MOSFET in snapback mode. As a result, Vdd stays relatively low <3.5V.

SPICE-Equivalent Circuit Analysis

In contrast to the above mixed-mode circuit-device analysis, conventional circuit simulation uses compact device models which do not take advanced physical effects into consideration. To isolate the important of these physical effects, we repeat the simulation summarized in Fig. 3, with impact ionization models turned off. Results of this comparison analysis are summarized in Fig. 3 (insert). Clear differences to the physically accurate results shown in Fig. 3 are evident.

Circuit Optimization

Physically accurate simulation provides an efficient tool for circuit optimization. As visible in simulation results in Fig. 3, the latch turns off at about t=60ns, causing the gate potential of the protection device M3 to drop. Even though this does not cause real problems because M3 remains in on-state with

strong bipolar conduction, operation of the circuit can be improved by allowing the latch to remain on longer.

To allow the latch to remain turned on after the node RC has discharged, we reduce the width of the pull-up device M4 in the inverter. Thus the inverter is still strong enough to force the latch into the on state, but not strong enough to force it off.

A final comparison of simulations results is shown in Fig. 4. The output voltage of the protection circuit Vdd is unphysically high (12V) for a SPICE-equivalent simulation (blue), physically accurate simulation shows that the protection circuit keeps Vdd below 3.5V (red) and a circuit modification prevents the latch from turning off and keeps Vdd even lower (green curve).

Conclusions

Physically accurate analysis of ESD protection circuits using mixed-mode circuit-device analysis software was demonstrated. It is shown that physical effects such as impact ionization and parasitic bipolar action are essential in the operation of MOSFET-based ESD protection circuits, including the use of triggering circuit. Conventional SPICE simulation, which does not consider impact ionization and other advanced physical effects, cannot provide sufficiently accurate analysis of these circuits and can lead to grossly inaccurate results and may cause costly design mistakes. Physical-level simulation is therefore required, such as shown in this work.

References

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[2] Michael Stockinger, et al., *"Boosted and Distributed Rail Clamp Networks for ESD Protection in Advanced CMOS Technologies,"* ESD/EOS 2003, Las Vegas, USA

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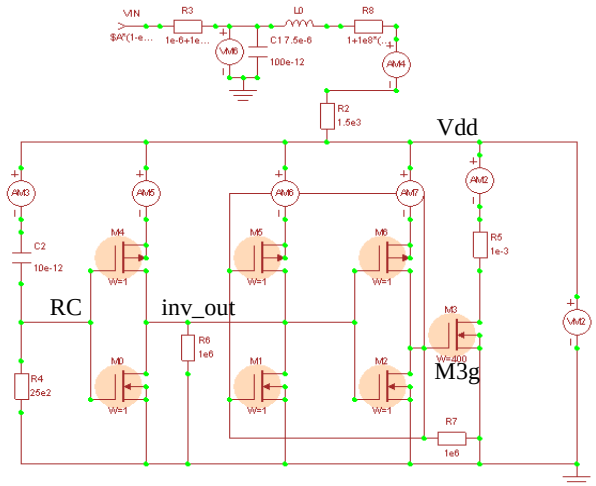

Fig. 1 Schematic of ESD protection circuit with feedback triggering mechanism [1].

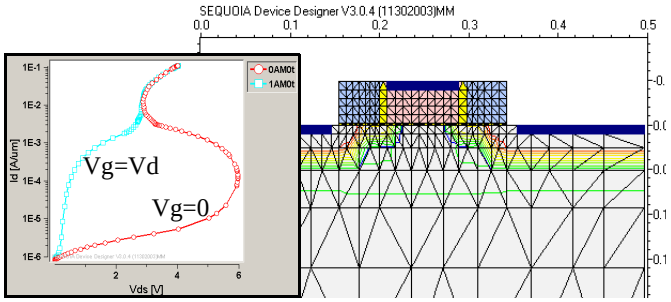

Fig. 2 FInite Element model of a 90nm n-type MOSFET generated using [3]. **Insert:** High-current drain curves in the grounded-gate configuration (red curve) and with the gate tied to the drain (cyan curve).

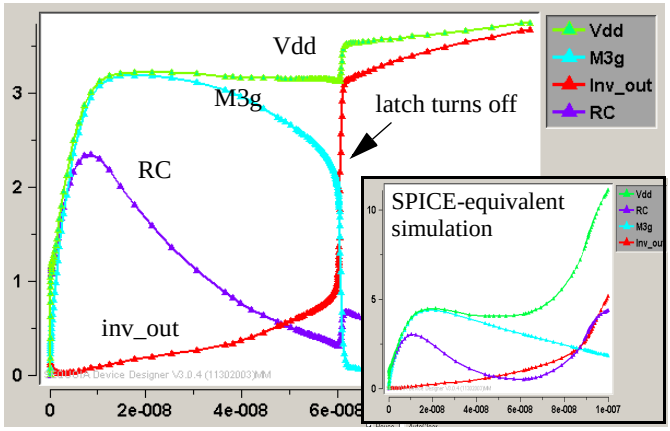

Fig. 3 Internal behavior of the protection circuit Fig. 1 under 2kV HBM stress. RC filter potential (blue) is elevated by the pulse for about 25ns. Inverter output (red) stays low during this time, causing the latch to stay on and keep the gate potential of the protection device M3g high (cyan). With M3g>>Vth, the protection device is on, keeping Vdd low (green). The latch turns off again at about 60ns, forcing the protection device to trigger. Parasitic bipolar current conduction keeps Vdd low even after the latch turns off. **Insert:** SPICE-equivalent simulation neglecting impact ionization. Clear differences to the physically accurate results are evident. The output voltage of the protection circuit rises as high as 12V.

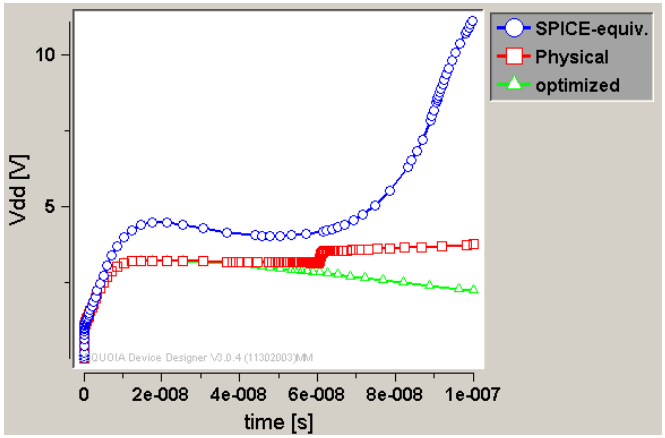

Fig. 4 Summary of Vdd simulation results: SPICE-equivalent simulation (no impact ionization) in blue, physical mixed-mode simulation in red, optimized circuit in green.