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Efficient Analysis and Optimization of ESD Protection Circuits

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Abstract

Electrostatic Discharge (ESD) is generally recognized as an increasingly important issue for modern integrated circuits. Thinner gate oxides, complex chips with multiple power supplies and/or mixed-signal blocks, larger chip capacitance and faster circuit operation all contribute to increased ESD-sensitivity of advanced semiconductor products [1]. Detailed understanding of complex circuit-device interactions is essential for the design of effective ESD protection. This paper presents results of an ESD failure analysis, where excessive distance between the IO pad and the power supply ESD protection can lead to permanent failure during ESD stress. The critical distance for a given protection type is calculated and remedies for the situation shown.

Industrial ESD Analysis

Although it has been long expected that simulation can and should play an important role in addressing ESD issues, industrial applications have been rare. The problem has been approached from two directions: circuit simulation with added empirical high-current device models [2] and device simulation with added mixed-mode simulation. The circuit simulation approach has suffered from its non-physical nature and poor convergence. The device simulation approach has been previously limited to few research-type aplications because of ease-of-use problems, meshing issues and excessive simulation run times.

This paper discusses an industrial application of a novel ESD simulation tool [3], which combines physical acuracy of mixed-mode circuit-device simulation with the usability of an integrated circuit designer package. The tool provides capabilities for in-depth studies of device-level effects [4],[5] as well as analyses of larger circuits characterized by complex interactions within I/O buffer circuits embedded in their chip environments and Charged Device Model (CDM) problems [6].

Numerical analysis of industrial ESD problems poses a number of specific challenges. ESD events push circuits into high voltage and high current operation regimes posing challenges for convegence, their high speed makes the incorporation of RLC parasitics important, and the distributed nature of many discharge events necessitates the inclusion of a substantial number of active and passive elements. Ease-of-use is a critical consideration for the acceptance of ESD tools, since ESD problems are typically addressed by design engineers and not a dedicated research group.

Device synthesis and automatic mesh generation are used in conjunction with inverse modeling to generate devices which assure accuracy and reasonable simulation times. These calibrated devices are stored in a library to be used by ESD circuit designers. The ESD-relevant circuit is specified through the built-in schematic capture tool, finite-element device models are imported from the device library.

IO Buffer and ESD Protection

The simulated ESD-relevant circuit is shown in Fig. 1 along with the device structure and mesh used for the protection clamp (insert). The mixed-mode circuit contains five active finite-element level devices (3 NMOS and 2 PMOS) as well as passive circuit elements. MOSFET widths are specified as in the layout (input CMOS pair with Wn/Wp=40μm/20μm, wider output MOSFETs Wn/Wp=200μm/100μm and a power supply clamp with Wn=400μm). A chip capacitance of 200pF and intrinsic Vdd and Vss resistances of 5Ω each are also included since both have a significant effect on circuit behavior during ESD stress. An HBM discharge circuit is included with a 100pF capacitor pre-charged to 2kV, 7.5μH inductor and 1.5kΩ resistor.

MOSFET breakdown behavior was compared to experimental data. Simulated curves shown in Fig. 1 demonstrate snapback for NMOS devices with triggering voltages around 9.5V. The P-MOSFET triggers at around 11V but does not enter snapback. This behavior corresponds to experimental data.

Figure 2 shows currents versus time for the clamp current AM2 and output buffer current AM9 for three different R6, R7 values: 1Ω, 2Ω, 4Ω. These resistors represent the electrical distance between the IO pad and power supply protection clamp M10 (Fig. 1).

A qualitative transition is seen between the values 2Ω and 4Ω. For 2Ω or smaller the entire HBM pulse is absorbed by the ESD protection device M10, while for 4Ω and larger the output buffer NMOS M13 triggers first and draws a current of about 0.17A. This current is high enough to destroy the IO buffer power supply tracks.

In cases when the output buffer NMOS triggers, a delay is visible in the triggering of the clamp M10 as shown in Fig. 2.

Lowering the Clamp Triggering Voltage

One possible solution to this ESD problem is to reduce the resistance between the IO pad and clamp. Another solution which may be preferable is to lower the triggering voltage of the protection clamp. A common technique to achieve this has been proposed in [7],[8]. It involves the addition of a capacitor between gate and drain of the clamp to raise the gate potential temporarily during the pulse. A drawback of this technique is the need to carefully optimize the circuit parameters to cover all relevant ESD discharge types. Simulation is an efficient tool for this task.

Our modified circuit is shown in Fig. 3. The added capacitor C2 and resistor R13 transform the ESD clamp M10 into a low-pass filter with an RC constant of about 7ns. The gate-source voltage of the clamp M10 rises above the MOSFET's threshold voltage (Fig. 3) causing the clamp to turn on. This is long

enough to allow the clamp to trigger well before the output buffer reaches its triggering voltage of about 9.5V and thereby keep the voltage across the protection clamp to a safe value (Fig. 3). As shown in Fig. 4, the addition of capacitor C2 fully protects the output buffer, which now does not trigger despite the large 4Ω resistance between IO pad and ESD clamp. The robustness of the protection scheme is thus increased allowing more flexibility in the placement of protection clamps.

Conclusions

We described a simulation procedure suitable to analyze ESD protection schemes, investigate ESD failures and optimize protection circuits. The application shown is the placement of power supply protection clamps, which must be sufficiently close to the I/O buffer to absorb the discharge energy and prevent triggering of the buffer MOSFETs. The maximum electrical distance between I/O and the protection clamp is calculated for a given protection scheme and MOSFET properties. A circuit solution to the problem is shown, which improves the protection capabilities of the power supply clamp without major changes to either circuit or front-end process.

References

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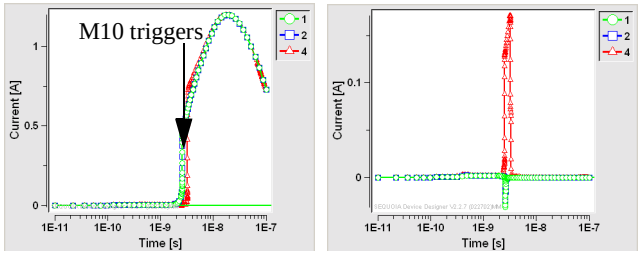

Fig. 2 Protection clamp current AM2 (left) and output buffer current AM9 (right) for track resistance values 1, 2 and 4Ω. The clamp triggers at around 2ns after the discharge starts. For resistance values of 4Ω or higher, output buffer MOSFETs trigger first with peak current reaching 0.2A, destroying metal lines in the buffer.

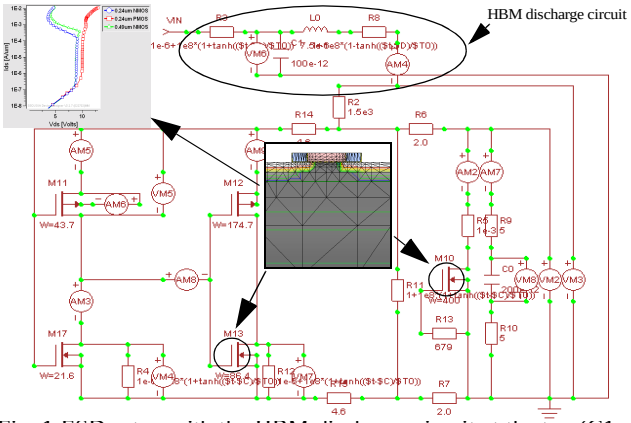

Fig. 1 ESD setup with the HBM discharge circuit at the top (C1, L0, R2), protection clamp M10 (L=0.49µm, W=400µm), chip capacitance C0 and output buffer. R6, R7 are power track resistances between the IO buffer and power supply protection clamp M10. FEM device structure used for MOSFETs is shown in the insert. Also shown are calibrated breakdown curves for several MOSFETs used in this work: Lpoly=0.24, 0.49µm NMOS, 0.24µm PMOS (no snapback).

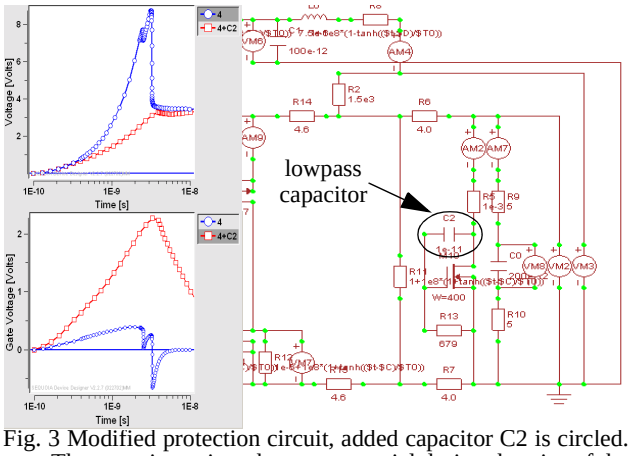

Fig. 3 Modified protection circuit, added capacitor C2 is circled. The capacitor raises the gate potential during the rise of the ESD pulse thereby lowering its triggering voltage.
Plot on left bottom shows gate-source voltage of the protection clamp M10 versus time with (red) and without (blue) capacitor C2. Gate potential is raised by C2 causing an early turn-on of M10.
Plot on left top shows voltage on the ESD protection clamp vs. time for the 4Ω case (blue circles) and added lowpass capacitor C2 (red squares, ESD clamp triggers early and protects the output buffer).

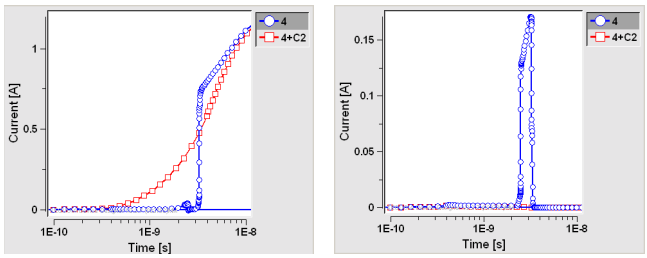

Fig. 4 Protection clamp current AM2 (left) and output buffer current AM9 (right) with (red) and without (blue) lowpass capacitor C2. Addition of C2 prevents triggering and protects the output buffer.