Statistical Aspects of Modern IC Designs

Valery E. Axelrad and John K. Kibarian
valerya@pdf.com, jkk@pdf.com
PDF Solutions Inc.,
333 W. San Carlos St., San Jose, CA 95110

1.0 Abstract

Increasing circuit complexity and die area with at the same time decreasing device dimensions render traditional approaches to IC design inadequate. The result is serious risk of suboptimal designs and thus poor performance and/or poor manufacturing yield. New tools are necessary to capture the effects of statistical variability of devices and interconnects on circuit performance. No longer can circuit design be carried out independently of the process design as interactions between the two cannot be neglected. This means redefining the conventional Mead-Conway design style which has served the industry so well in the past. A new design-manufacturing interface is described and a few challenges and solutions are shown.

2.0 Introduction

The challenges and rewards of designing and manufacturing leading edge integrated circuits have scaled with the complexities of chip functionality. Once a commodity industry for the larger electronics systems business, the semiconductor business has grown faster than its parent industry as the semiconductor fraction of system value has increased. Most of this growth is a natural extension of Moore's famous law which states that the density of integrated circuits would double every 18 months. Today, the IC business is a $150B industry which supports the $750B electronics industry.

With so many peoples' fortunes tied up in the industry, the question arises how much longer Moore's Law can be maintained. Recently Dr. Moore addressed this issue at the Electro-Chemical Society Meeting. While optimistic about the short range future, he discussed several of the key hurdles related to increasing variability of active and passive circuit components which must be overcome through the use of statistical design and of mask manipulation techniques (such as optical proximity correction and phase shift). These techniques allow to consider increased process variability during the design.

Such techniques seem to run counter to another industry paradigm: The Mead-Conway Design method [1]. Simply stated, the Mead-Conway method tries to establish a simple interface between the process and the design. It enabled the growth of fabless semiconductor companies and has made concurrent process and product design possible.

In this paper, we will discuss the following:

- The conventional interface between design and manufacturing

- The technology forces which drive the need for considering process variations during the design phase
- A proposed new model for the interface between design and manufacturing
- The challenges to the implementation of such a model and possible solutions
- Examples of the new interface
- Conclusions

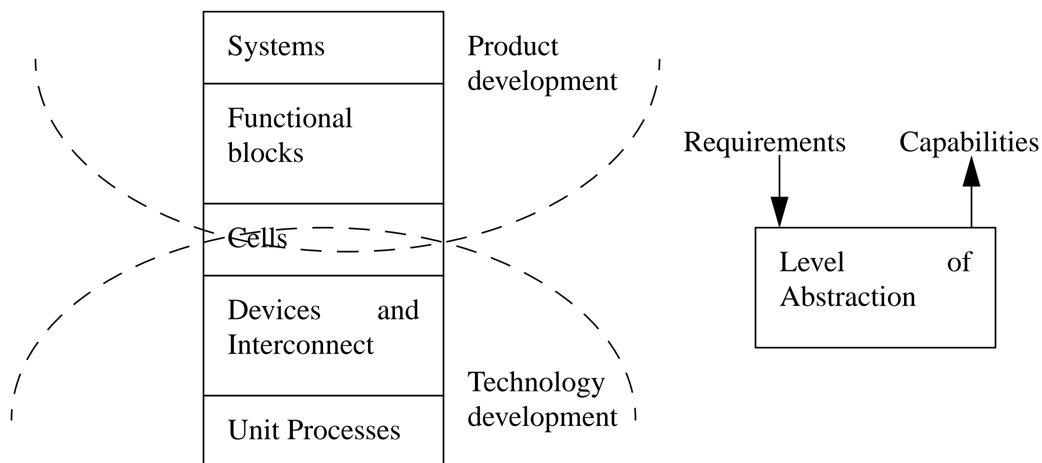
3.0 Overview of the Design-Manufacturing Interface

A large number of engineers are involved in the development of an integrated circuit from unit process development to system specification. At each level of abstraction, engineers are given requirements and determine capabilities as shown schematically in Figure 1. For many reasons, development has been split into two basic areas, product development and process development. Three aspects of technology and product development are particularly relevant to this paper:

1. Many products are usually manufactured using the same process
2. Process and product development are often undertaken at different companies
3. Product performance variability and yield are determined by its sensitivity to the intrinsic variability in the process.

While a product's functionality is often statically defined during development, the process will vary during manufacturing. In the early 1980's the advent of very large scale integration created the need to formalize the interface between design and manufacturing. To simplify the boundary between the product and process development areas, semiconductor companies standardized on a basic interface of SPICE model cards and LPE/DRC technology files. Using this interface to simplify the design problem is commonly referred to as the Mead-Conway [1] design methodology.

Figure 1. Layers of development for an IC



The advantage of this type of interface is that the product and process design can be decoupled and even performed concurrently. There are however two disadvantages:

1. The flow of information from the process developer to product designer is uni-directional and is assumed to be static

   -> It is assumed that the choices the designer makes have no impact on the electrical performance of the fundamental elements (e.g., transistors and interconnect structures) used in the design.

2. Conservative specifications of the process are provided to the product designers

   -> This results in losing much of the potential performance improvement of the new process technology due to guard banding.

These two negatives have long been outweighed by the value in disaggregating the technology development from the product development for most product segments, especially ASICs and most logic products. On the other hand, memory and mixed signal chip designers have often employed design methodologies which use more information about the process.

We believe that this is changing. The changes are going to require re-defining the interface between design and manufacturing while still maintaining a clean interface which allows for the disaggregation of design and production. It will create opportunities in the mixed signal and memory area enabling a more efficient design style, while providing the logic designers with an ability to understand what is happening on the other side of the interface. Most of these changes are due to the evolution of process technology. In the next section we will outline some of these and document them with examples.

4.0 Manufacturing Evolution

To support Moore's Law of doubling performance every 18 months, the size of a die has increased approximately 40% per generation. With recent generations this has been supported by the application of single wafer processing equipment, large NA steppers, and CMP processing. Over this period, the within wafer and within chip sigmas for key device and structural measures (e.g., CDs, ILD thickness, etc) have become a significant portion of the total process variability.

For years, IC engineers have known that the matching of two transistors on a chip is a function of the distance between them and the area of the transistor structure. This is phenomenologically captured in Pelgrom's law which equates matching to distance and area. Memory and mixed signal design engineers have accounted for these problems by compromising area for matching. Logic designers have had the luxury of ignoring this problem and only investigated circuit performance using worst case model files. In this type of analysis, the unstated assumption is that within die variation is not a problem.

In recent years, it has been demonstrated that the amount of within chip variation of key device parameters is becoming a significant portion of the total device variability. Moreover, while random spatial variations are captured with phenomenological models such as Pelgrom's model [2] , recent work suggest that spatial variations typically have a large deterministic component which-

depends on the layout of the chip. This is summarized in the table shown below and details are provided in the next subsections.

TABLE 1. Changes in IC technology and the implication for design-manufacturing interface

Change	Implication	Pressure on interface
Approaching resolution limits of photolithography systems and etch	Larger within chip variations of device gate length and metal widths	Static worst case models and simple technology files not sufficient to capture technology for design
Increasing number of metal layers	Increased emphasis on Chemical Mechanical Polishing (CMP)	Actual dielectric thickness (and hence capacitance) a function of specific layout.
Transistor gate length approaching 1000 Angtroms	Small number of dopant atoms actually in channel	Large fluctuation in device performance

In summary, there are three important conclusions:

1. Within chip variation is becoming a large portion of total device variability
2. Some of the within chip variation is deterministic and can be modeled (i.e., not random)
3. To predict within chip variation one must know the mask layout for the entire chip and the equipment characteristics.

4.1 Increased Within Chip Variability of Linewidths

There have been many studies of the variability of printed lines for deep submicron printing processes [3][4][6][9]. These studies show that the within chip sigma of most processes is approximately 60% of the process level variability. Moreover, for each generation of lithography technology the within chip variation becomes a larger percentage of the total variability. While this is the case for all layers, it is particularly true for the poly layer since it typically dominates the Leff variation of transistors and hence the drive currents. The within chip variation is typically due to effects such as micro-loading in the etch, variation in photo resist thickness, optical proximity effects, and stepper within field aberrations. Most of this variation, while spatially dependent, is not random and can be predicted based on an understanding of the lithography, photo resist development etch processes and the actual mask set used. As an example Figure 2 from [6] shows the simulated gate length variation of an SRAM macro cell implemented in a 0.25µm technology using a DUV 248 nm stepper. For the circuit in this example [6] the intra-die gate length variation results in a significant amount of skew in signal arrival times.

4.2 Increased Use of Chemical Mechanical Polishing (CMP)

While CMP planarizes the dielectric, the amount of material removed is highly dependent on the pattern density of the under layer [5]. As a result, the dielectric thickness variation within a chip can be thousands of angstroms. Typically, the within chip variation is larger than the within wafer variation. Like the poly critical dimension variation, most of the within chip variation in not purely random but depends on the layout, CMP pad material, slurry chemistry, rotation rate, and down force applied.

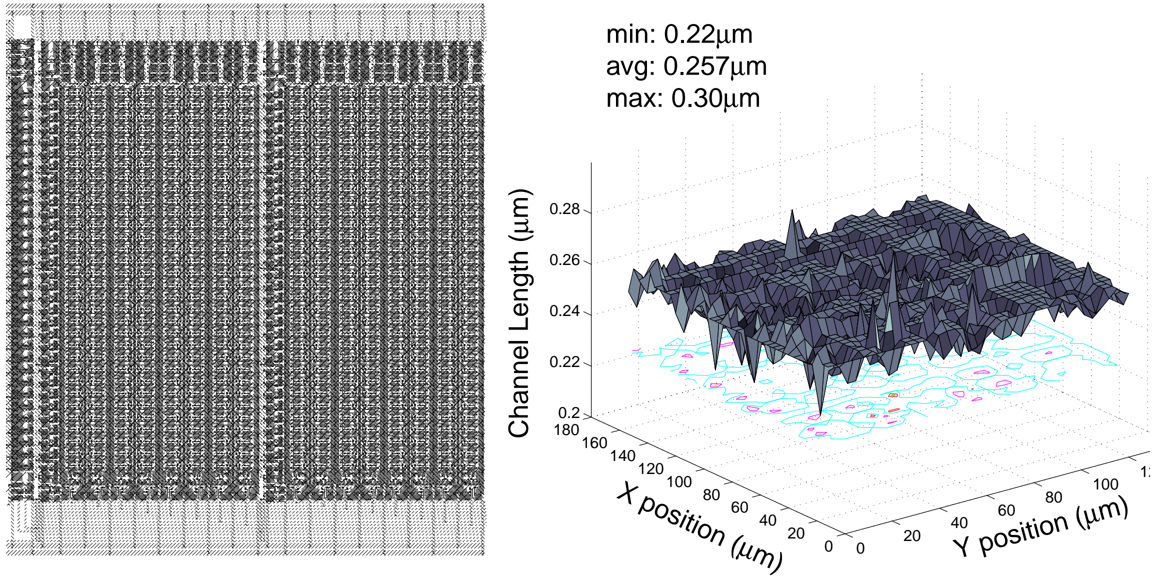


Figure 2. Simulated intra-die poly-CD variations in a 0.25µ design rule SRAM macro cell (from Stine et al. [6]).

4.3 Threshold Variation Due to Spatial Fluctuation of Channel Doping

Statistical fluctuations of the dopant concentration are an increasingly significant source of active device variability. With decreasing device dimensions the number of dopant atoms in the active volume is dropping into a range where the variability due to sample size becomes substantial. As an example, consider a MOSFET with the effective channel length of 0.1 microns. The electrically active volume can be estimated to approximately: Leff*W*Dch (Dch is the thickness of the inversion layer, for modern devices approximately 0.01µm). With estimated values for Leff, W, Dch and Nch (channel doping) the active volume contains about 500 dopant atoms (EQ 1). The actual number of atoms is subject to statistical fluctuation on the order of $1/\sqrt{SampleSize}$. Therefore the statistical fluctuation of the threshold voltage and the drain current is on the order of 4% (EQ 2). This variability is in the range of gatelength variability (Poly CD variation), which is typically as large as 10%.

$$L_{eff} \cdot W \cdot D_{ch} \cdot N_{ch} \approx 0.1\mu m \cdot 0.5\mu m \cdot 0.01\mu m \cdot 10^{18} cm^{-3} = 500 Atoms \qquad \text{(EQ 1)}$$

$$\sigma_{IDsat} = \frac{1}{\sqrt{500}} = 0.04 \qquad \text{(EQ 2)}$$

5.0 New Model for the Design-Manufacturing Interface

As we demonstrated in the previous section, there are three trends which are driving IC designers to reconsider the conventional design-manufacturing interface. The new interface needs to provide the following information to the designer:

- The intrinsic electrical variability of the circuit elements such as transistors and interconnect structures due to process variations

- The sensitivity of the electrical characteristics of circuit elements to choices made by the designer (e.g., the impact of layout configuration on electrical performance of interconnect).
- Post design manufacturability assessment and post design printability improvement [7].

We have shown this graphically in Figure 3. The interface is referred to as a parameterized one

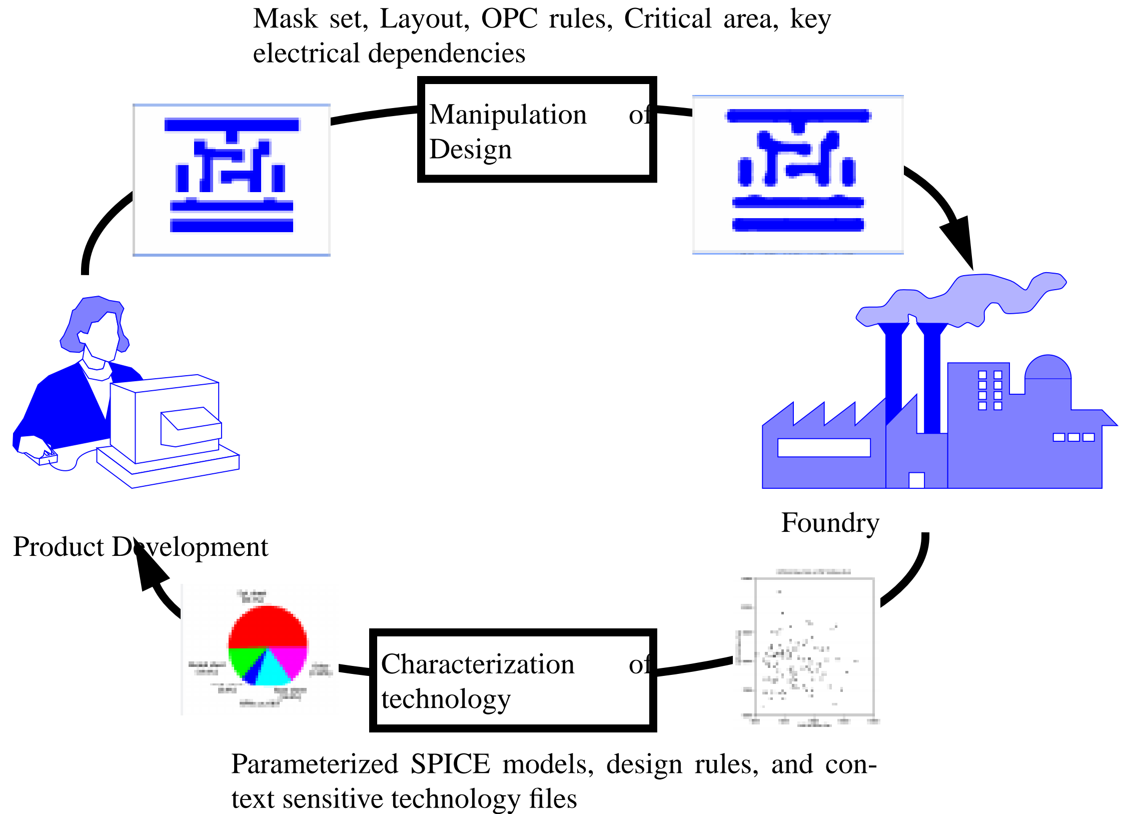


Figure 3. An active bi-directional interface which parameterizes the information transferred

because designers can query how changes to the structure will impact electrical performance. For the remainder this paper we will not focus on the changes to the design and manufacturing evironments because we believe these are mostly incremental beyond present capabilities. We will instead discuss how TCAD can play a role in the parameterization of the interface between design and manufacturing..

6.0 Challenges and Solutions for the New Interface

As we pointed out in the previous section there is a need to preserve a clean interface between the design and the manufacturing while allowing for the parameterization of a new technology. In addition to accuracy, there are two conditions which must be met.

1. It must be possible to characterize the process early in the lifetime of the new technology
2. It must be possible to characterize the effects of small perturbations

To meet these two conditions we believe that TCAD is evolving from being mostly used for technology research and development to a tool used to help build a bridge between design and manu-

facturing. While the predictability of TCAD when used for development of entirely new technologies has been problematic, it is often an excellent tool for predicting the effect of small perturbations.

For TCAD to be adopted for the role of parameterizing the interface between design and manufacturing, several hurdles must be overcome. The solution artefacts must be kept well below the variability of electrical characteristics due to simulated process variation. In this paper we have discussed the broad issue of the interface between design and manufacturing. While this interface includes many technologies where TCAD will be important such as the post layout printing correction (referred to as OPC) and interconnect characterization, for the remainder of this paper we will focus on the issue of capturing the intrinsic variability of the active devices due to process variation.

There are four necessary conditions to apply TCAD to the task of statistical SPICE parameter characterization:

- Ability to predict the distributions of electrical test values and SPICE parameters based on the distributions of equipment controls

  This mapping of distributions can be performed in a number of ways. When the expected distributions are highly non-linear (as they are for SPICE parameters which model complex effects such as subthreshold characteristics of a MOSFET), the most accurate way to accomplish this mapping is through Monte Carlo simulations. This has been demonstrated in numerous papers [18][20][21][23][24][25].

- Ability to use deterministic algorithms when extracting SPICE parameters

  SPICE models are highly non-linear equations. The traditional way to fit these equations is via gradient based optimization. Since the objective function is complex, the solution is not unique, and hence not necessarily physical. The result is that while the fit is typically very good, if this procedure is applied to hundreds of devices to determine the effects of process perturbations on SPICE parameters, the obtained correlations tend to be difficult to interpret and are often not physical [20]. As shown in [20], it is possible to use the information available from TCAD process simulations (such as actual dopant profiles) to extract the SPICE parameters in ways which cannot typically be accomplished from I-V characterization.

- Ability to reduce a large distribution of SPICE parameters to an analytical model suitable for use inside commercial SPICE packages, which captures the variability of SPICE parameters due to both deterministic and random variations in the process. This is possible using advanced algorithms based on the Principal Component Analysis [10][11], i.e. an eigenvalue/eigenvector decomposition of the correlation matrix [18]. Principal Component Analysis allows to extract the underlying basic variables from the typically much larger number of correlated observables. Traditional PCA expresses SPICE parameters in terms of arbitrary random variables which have no physical meaning. For PCA-based algorithms to be useful for IC designers the software must interpret these factors and model the SPICE parameters in terms of E-tests [20].

- Ability for the TCAD process and device simulators to perform an accurate transformation from process conditions to transistor characteristics.

  It is well known that the accuracy and robustness of the results of process and device simulation is highly dependent on the mesh used. Since different partial differential equations are solved for both the process and device, different discretization meshes are needed for each. This problem has been a limiter in the ability to predict the effects of small variations on device perfor-

mance. The typical conventional solution is to use a very conservative mesh, which costs CPU time and makes Monte Carlo simulation too time consuming. We believe however that progress has been made with respect to this topic.

6.1 Improving the Robustness of TCAD through Mesh Optimization

Robust triangulation of complex device structures in particular at the interface between multi-dimensional process and device simulation is a problem universally recognized as a potential show-stopper in TCAD. Triangulation in TCAD is critical for several reasons: computational efficiency and robustness favor well-shaped elements and small node counts. Accuracy dictates placing dense anisotropic regular layers of elements at junctions and inversion layers. The accuracy requirements become particularly important for statistical TCAD applications, where gridding noise can overpower useful information. To keep such noise low, special care must be exercised in the gridding process.

The conventional approach to multi-dimensional integrated TCAD is to use the same triangulation for both process and device simulations. The needs of the device simulation thus are incorporated into the mesh utilized during the process simulation. This mesh is a "compromise" one, which is typically very large and frequently of poor quality. As a result, mesh sizes on the order of 3000-7000 nodes for a submicron MOSFET and even larger for complex power devices are common, leading to very long simulation times and in some cases convergence problems (particularly with large isolation structures and power devices). Statistical applications of TCAD where a large number of simulations are required to sample the design space further aggravate this problem [14].

This problem is addressed by a recently developed mesh generation algorithm. The algorithm preserves the complexity of the original structure while allowing precise placement of mesh nodes and lines at the locations required for accurate device simulation. The remeshing procedure decouples the process simulation mesh from the device simulation mesh. As a result, both can be made much smaller without loss of accuracy allowing a dramatic speed-up of the overall simulation (typically 5-25 times).

6.2 Robust Meshing for Complex Structures

The new algorithm has been implemented in a tool called pdMesh [10],[13],[14]. The fundamental strategy of the proposed method is to place mesh nodes and element edges in the simulation domain according to the application-specific needs of the problem and then connect them to a Delaunay mesh using a robust triangulation engine [15]. The main characteristics of the approach are as follows.:

- Use of a powerful extension language (Tcl) to adapt to particular device types and specific requirements to the mesh to be generated. Layers of mesh nodes can be placed explicitly where they are needed.
- Original material boundaries as generated by the process simulator are preserved. Only modifications to boundaries as requested by the user in the Tcl control file (device-type specific meshing template) are performed. These can include refining and unrefining the boundary. Complex geometries do not pose a stability problem as commonly observed with quad-tree based algorithms.

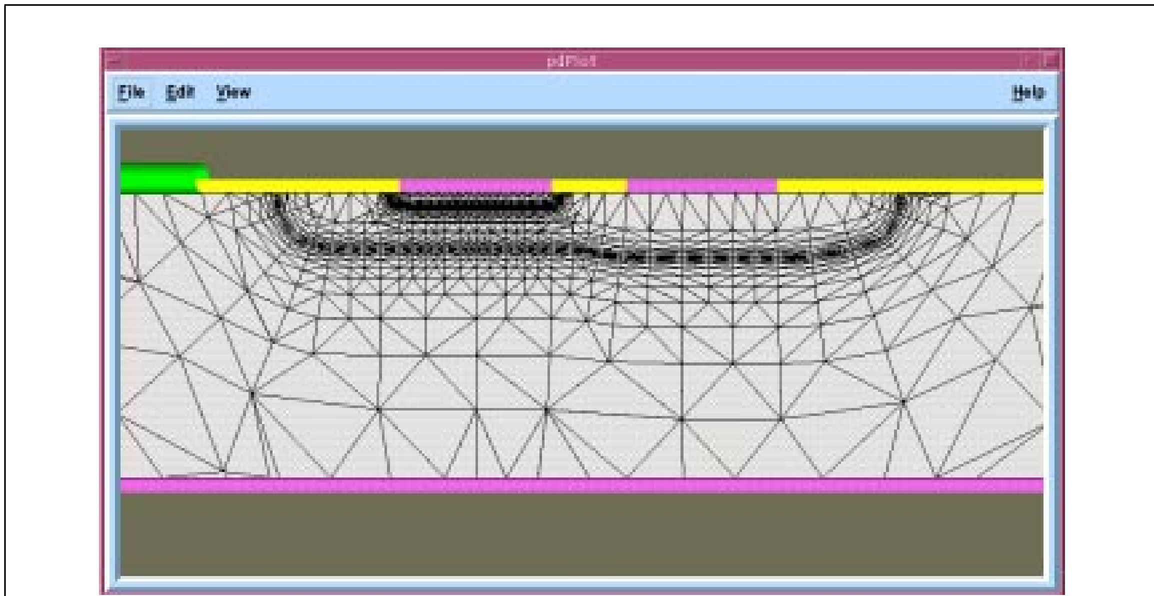


Figure 4. A BJT mesh created with pdMesh

- Layers of mesh nodes can be placed along material interfaces (for MOS channels) and along any contour of an analytic expression (e.g. a pn-junction, a certain doping value, equipotential line, etc.) This allows the user to adapt the mesh to both the particular geometry and a previously obtained process or device simulation result.
- Highly anisotropic meshes can be created, which are essential to treat inversion layers, pn-junctions, etc. As examples Figure 4. shows a BJT mesh and Figure 7. shows a MOSFET mesh

6.3 Application Example of the Meshing Algorithm

An industrial application is used to demonstrate the new algorithm in a realistic setting. The device is a 0.35 micron PMOS developed by a major US semiconductor manufacturer. The process was simulated with TSUPREM-4 [16] using a "compromise" initial mesh designed to provide sufficient resolution for the subsequent device simulation. The resulting mesh has 7600 nodes and is shown in Figure 6. A new mesh generated by pdMesh is shown in Figure 7. As seen in Figure 7. mesh layers were placed in the channel as well as in the junctions of the device. A vertical channel mesh resolution of 2nm is achieved despite an overall low node count of 1400. This channel mesh spacing was chosen to match the channel resolution of the reference TSUPREM-4 mesh (Figure 6.). To validate the quality of the new mesh in comparison to the original one, a gate curve (Id vs. Vg) was generated using both structures and showed less than 0.1% difference in Vth (see text below Figure 6., Figure 7.). The two gate curves are almost identical as shown in Figure 5. A comparison of CPU times as shown below the Figures indicates a speed-up of about 20 times.

The new meshing procedure was shown to dramatically improve TCAD simulation speed and accuracy by decoupling the device simulation mesh from the one used in process simulation. The algorithm creates highly anisotropic mesh layers which resolve channels, pn-junctions, etc. The resulting mesh respects the original geometry and is adapted to the physics of the device under consideration.

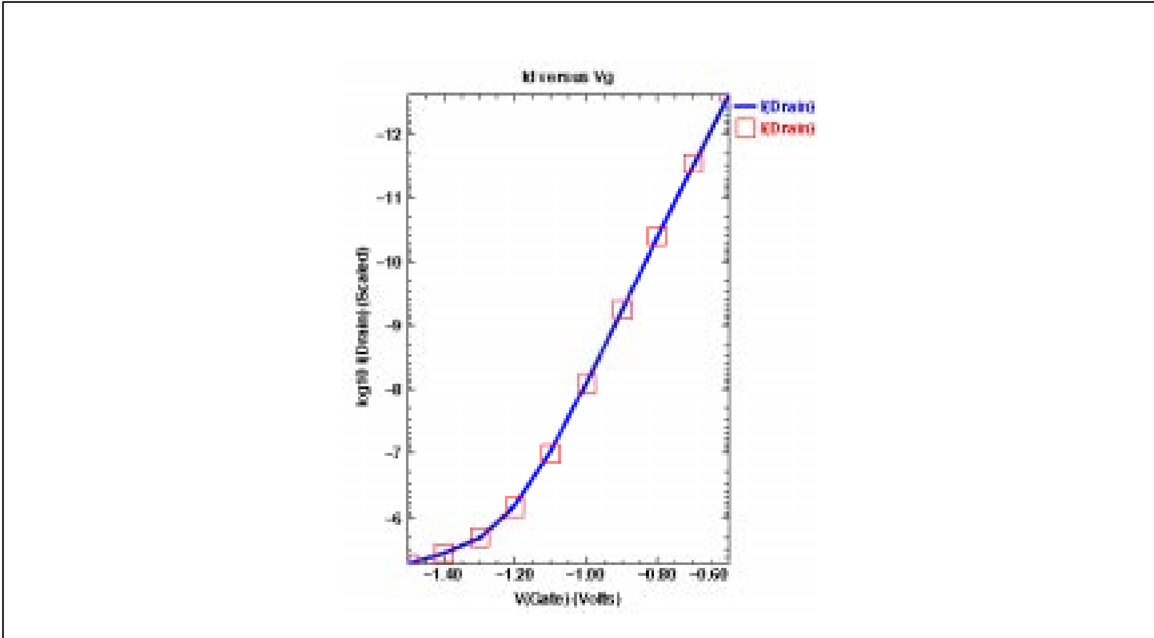
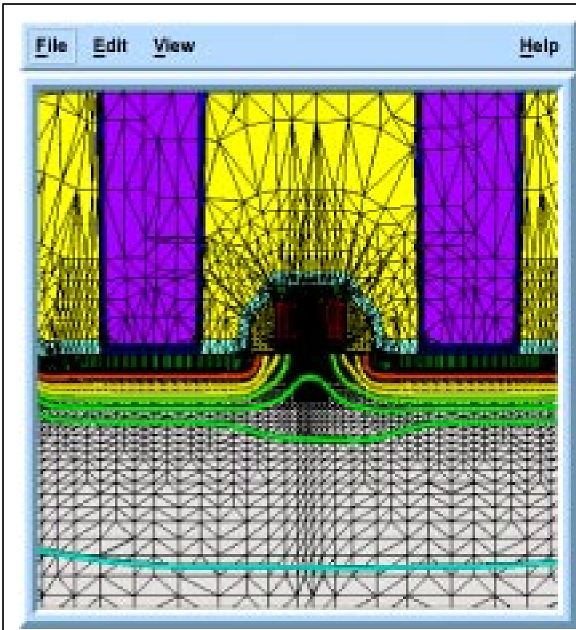
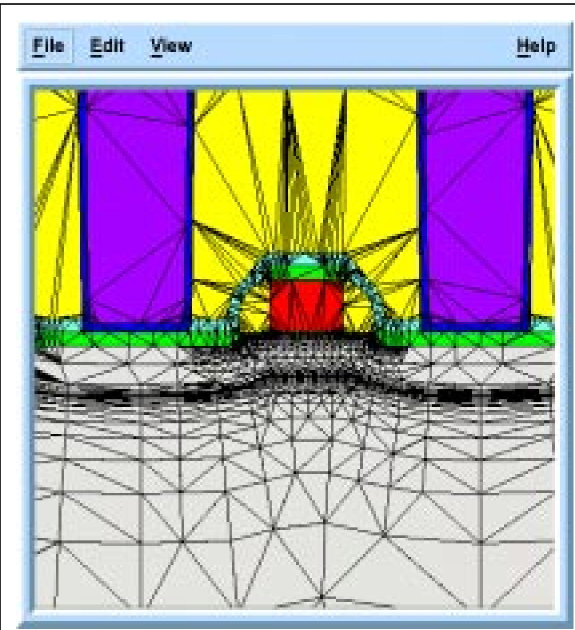


Figure 5. Id versus Vg data generated with both meshes: squares using the original mesh, solid line using the new pdMesh-generated one.



Vth=-1.171V, 30 min (UltraSparc1, Id vs. Vg)

Figure 6. Original TSUPREM-4 structure and mesh



Vth=-1.172V, 1.3 min (UltraSparc1, Id vs. Vg)

Figure 7. New mesh generated by pdMesh

7.0 Conclusions

Technology evolution is increasing the ratio of within chip variation to total process variation of key electrical performances of active and passive circuit components (transistors, interconnects,

etc.). The result is that the simple conventional interface between the design and manufacturing will not be sufficient in the future. We believe that the new paradigm will be a parameterized interface which will provide both sides with an understanding of how choices they make affect the overall chip performance, reliability, and yield. For our belief to materialize, TCAD will be used in new ways. This will place new and more strict requirements on the TCAD tools. One such issue is that of robust meshing. We believe that progress has been made in this area.

The changing interface requires R&D in several areas including:

- Parameterization of within chip variations of interconnect variability
- Ful chip post layout printability evaluation and enhancement
- Enhancement of design systems to exploit the additional information collected about the process
- Exploitation of circuit/process co-design

As this new interface is created and explored, TCAD tools will find a new relevance in the IC design community. We believe that this will create new opportunities for innovation for TCAD research and development engineers.

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