A Simulation Study of CMOS Performance Improvement by Laser Annealed Source/Drain Extension Profiles

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Abstract — **Laser Thermal Processing (LTP) dramatically changes the feasibility of ultra shallow and highly doped Source-Drain Extensions (SDE). In comparison to conventional Rapid Thermal Processing (RTP) profiles, steeper profiles and higher peak concentrations are achieved. This is of particular importance for sub-100nm devices, where limited steepness of RTP profiles can result in significant source-drain resistance (Rsd) and severe short-channel effects. In this work we demonstrate that LTP technologies can reduce the source/drain resistance Rsd by more than 70% for Lpoly below 100nm in both NMOS and PMOS. This leads to increases in saturation currents by up to 10%. Significant improvements in very deep submicron MOSFET performance can thus be expected as a result of this new technology being deployed.**

I. Introduction

In order to continue CMOS device scaling and improve device performance beyond 0.13 µm device node, shallow (Xj<30 nm) and abrupt junctions (Xab <3nm/decade) with low sheet resistance (Rs <300 ohm/sq) are required for the source and drain extensions [1]. These junctions are needed to reduce the parasitic resistance in the source and drain regions, in particular the spreading and accumulation resistance [2]-[4]. The main process challenges with junction scaling are the formation of abrupt and low sheet resistance junctions. In conventional implant and thermal annealing low sheet resistance is limited by solid solubility while abruptness is limited by implant and diffusion mechanisms. For B (i.e PMOS) these are more severe than As (NMOS). For example: for As typical junctions of Xj;Rs;Xab =300Å;300ohm/sq;<3nm/decade were achieved, while for B typical junctions of 300Å;900ohm/sq;8.5nm/decade were achieved. Advances in annealing using laser thermal annealing have shown significant improvement in reducing both sheet resistance and in forming highly abrupt junctions [5], meeting technology roadmap requirements.

In this study we used SEQUOIA device simulation to study the effect of junction steepness and dopant concentration in the source drain extension on the transistor drive current for Lpoly<100 nm. We compared junctions formed with low energy implants but annealed either with spike annealing or laser annealing.

II. Laser Thermal Processing (LTP) Technology vs. Conventional RTP

Fig. 1 shows typical SIMS profiles obtained with low energy B implants followed by either RTP or LTP anneals.

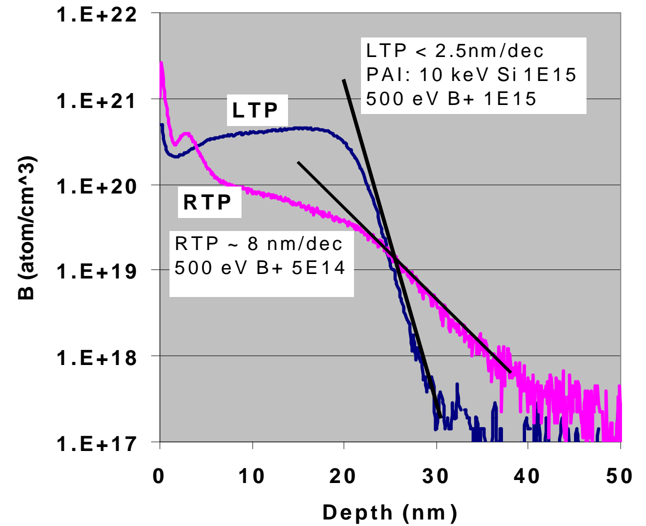

Fig. 1. RTP and LTP profiles (SIMS measured).

The RTP profile was obtained following 500keV B implants to 5E14 cm^{-2} and spike annealing to 1050 C (ramp up rate 250 C/sec). For the LTP profile a pre-amorphization implant (PAI) using 10 keV Si 1E15 was done before a 500 eV B 1E15 cm^{-2} implant. The wafer then was annealed using a laser energy of 0.44 J/cm^2, which resulted in melting the implanted area and activating the dopants. In LTP the junction depth is defined by the amorphous thickness formed by the PAI implant. The LTP gives a box-like profile with a steeper (<2.5nm/decade) junction and higher surface dopant concentration (>5E21 cm^{-3}) than the RTP profile (Fig. 1). Actual steepness of the LTP profile could be higher than shown in Fig. 1 due to limitations of SIMS resolution.

III. Simulation Methodology

A synthesis approach was utilized for a performance evaluation of RTP and LTP technologies. Devices were created using the SEQUOIA Device Designer software [6] to match experimentally observed SDE profiles and other known geometric features such as Lpoly, Tox, etc. SDE profiles are described by EQ. 1 and illustrated in Fig. 2. Parameters ‘Pow’ and ‘Ychar” were adjusted to match SIMS data, the ratio ‘XY’ between vertical and lateral profiles was chosen to be 0.7 [7]

$$N(x, y) = N \cdot \exp\left(-\left(\frac{y - y_{peak}}{y_{char}}\right)^{Pow} - \left(\frac{x - x_{peak}}{XY \cdot y_{char}}\right)^{Pow}\right) \qquad \text{(EQ 1)}$$

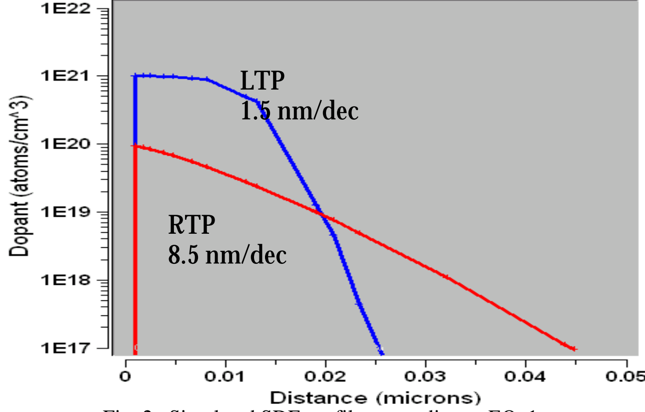

Fig. 2. Simulated SDE profiles according to EQ. 1.

An analytic description of the profile provides an excellent match to SIMS data and allows a clean comparison between RTP and LTP technologies. Process simulation was not utilized since to our knowledge reliable models for sub-100nm device nodes do not exist.

IV. Comparing Nominal Length Devices

A. *Device Structures*

For our comparison of LTP vs. RTP devices we adopted the following methodology:

- a device structure was designed with Lpoly=100nm, Tox=20Å, SDE with a lateral steepness of 8.5 nm/dec (RTP) and peak concentration of 1e20 cm^{-3}, 25nm Gate/Drain overlap [7] and a leakage current of Ioff=3nA/µm at Vdd=1.2V (Fig. 3, left)
- the SDE profile was modified for a lateral steepness of 1.5nm/dec (LTP) and a set of peak concentrations 1e20 cm^{-3}, 5e20 cm^{-3},1e21 cm^{-3}. SDE junction depth was adjusted for each to match specified Ioff=3nA/µm [1] (Fig. 3, right)

B. *Electric Potential Contours in On-State*

Electric potential contours calculated for the RTP/LTP devices (Fig. 4) show that voltage drop in the source-drain extensions is reduced with the LTP profile. Lowered source/drain resistance and therefore improvement in overall device performance can be expected. The actual performance improvement will depend on the obtained reduction in Rsd/Rtot — the ratio of source/drain resistance to total MOSFET resistance.

C. *Performance Improvement*

Current drive improvement due to the use of LTP is demonstrated by the set of output characteristics (IdVd curves) for the nominal length devices shown in Fig. 5. A summary of observed device properties is shown in Table 1 (L_{MET} is the metallurgic junction spacing at the oxide interface).

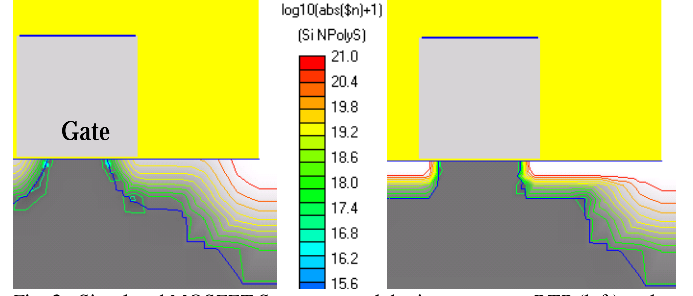

Fig. 3. Simulated MOSFET Structures and doping contours: RTP (left) and LTP (right).

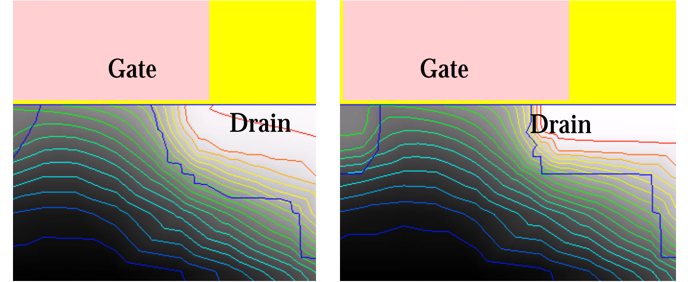

Fig. 4. NMOS electric potential contours in saturation near the drain corner: RTP (left) and LTP (right).

V. Device Performance Under Manufacturing Variations

Intrinsic limitations in semiconductor processing cause uncertainties in transistor geometry and doping profiles and thus an inherent variability in the electrical parameters of manufactured devices. This variability plays an important role in circuit performance and yield and is therefore of the utmost importance. CD control in photolithography is typically the

TABLE 1. ID_{SAT} [MA/MM], L_{MET} AT LPOLY=100NM

SDE Type	NMOS			PMOS		
	Id_{sat}	ΔId_{sat}	L_{MET}	Id_{sat}	ΔId_{sat}	L_{MET}
RTP	0.793	—	49	0.322	—	53
LTP 1e20	0.819	3.3%	65	0.332	3.1%	65
LTP 5e20	0.856	7.9%	66	0.340	5.6%	67
LTP 1e21	0.861	8.6%	67	0.342	6.2%	67

main source of device variation. As a result, device sensitivity to gate length variation is an important measure for judging the merits of a transistor technology.

A. *MOSFET Universal Curves*

MOSFET universal curves are a common metric for the evaluation of transistor technologies under gate length variation. Fig. 6 shows the saturation current versus leakage current in a device with gate length as parameter. Relative location of universal curves for different transistor technologies is commonly used to judge their respective qualities.

Changes in the universal curve are observed due to a reduction of source/drain resistance with LTP technologies illus-

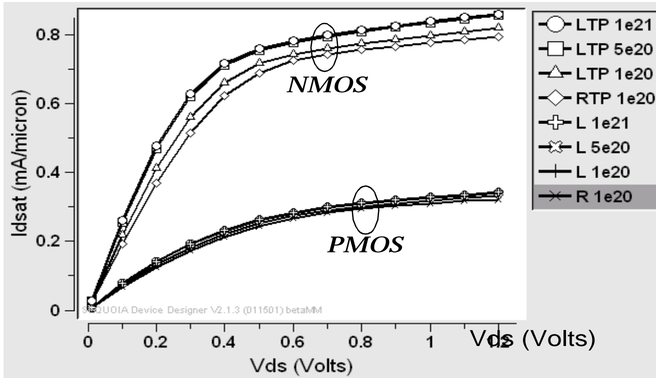

Fig. 5. Output characteristics at Vgs=Vdd=1.2V

trated in Fig. 7 and Fig. 8 Significant performance improvement is achieved as a result of increased lateral profile steepness (RTP vs. LTP 1e20). This is consistent with results reported by others [10]. Additional performance improvement is observed with increased peak SDE concentration from 1e20 to 5e20. A further increase in peak concentration is not as effective (see also Table 1).

B. PMOS Results

Similar results are obtained for P-channel devices as shown in Fig. 9 and Fig. 10, although the actual performance improvement achieved through the use of LTP is less pronounced than for the NMOS device shown in Fig. 6.

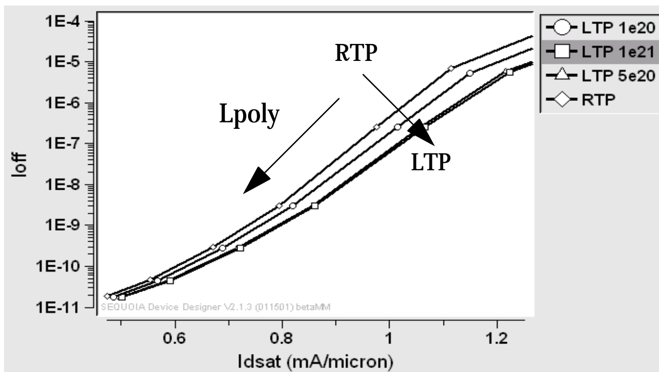

Fig. 6. NMOS Universal Curves, Ioff (A/micron) vs. Idsat (mA/micron).

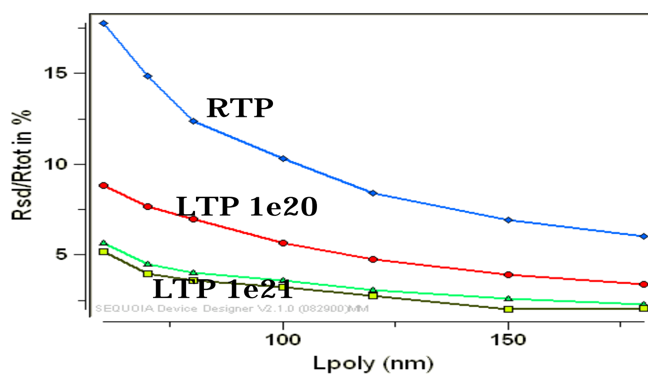

Fig. 7. NMOS Source/Drain resistance as percentage of total device resistance in saturation vs. Lpoly

VI. Further Scaling to Lpoly=60nm

Further device scaling below 100nm gate length can provide additional improvement in device performance. In this context it is interesting to examine the expected importance of SDE profile steepness. We scaled the device by reducing its gate length to 60nm, adjusting the channel doping to 1.5e18 and reducing Vdd to 1.0V [1]. SDE junction depth was adjusted to again match the specified leakage current constraint of 3nA/µm. Since the X/Y ratio of the SDE profile (EQ. 1) was kept constant at 0.7, the gate-to-drain overlap was thereby reduced to 16nm (RTP) and 10nm (LTP) [10].

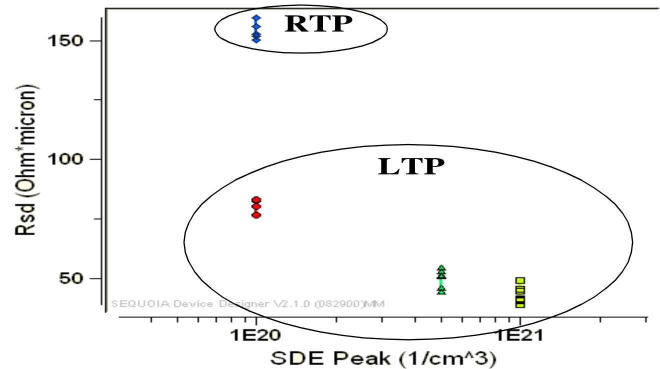

Fig. 8. NMOS Source/Drain resistance as a function of peak SDE concentration for RTP and LTP.

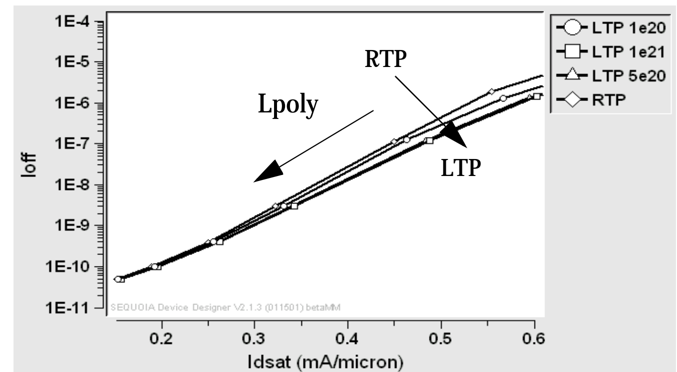

Fig. 9. PMOS universal curves, Ioff (A/micron) vs. Idsat (mA/micron).

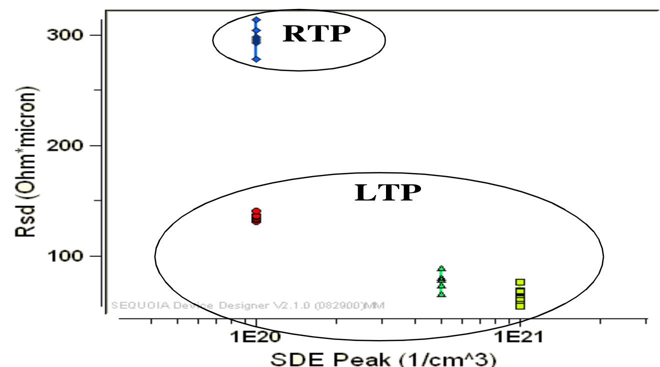

Fig. 10. PMOS Source/Drain resistance as a function of peak SDE concentration for RTP and LTP.

A. *Oxide Thickness Considerations*

The main improvement achieved by steeper SDE profiles is due to reduced source/drain resistance Rsd. For Rsd to have a significant effect on overall device performance, it must be a substantial fraction of overall device resistance. As shown in Table 2, this may not be the case unless it becomes possible to reduce the SiO_2-effective oxide thickness below 20Å.

B. *Universal Curves (Idsat vs. Ioff)*

As shown in Fig. 11, significant improvement can be observed for the Lpoly=60nm, Tox=10Å devices. Interestingly, a reduction in Lpoly does not guarantee improved MOSFET performance. It is necessary to also reduce Tox to compensate for the decreased Vdd, decreased SDE junction depth and increased channel doping.

TABLE 2. ID_{SAT} [MA/MM], L_{MET} AT LPOLY=60NM

SDE Type	**Tox=20Å**			**Tox=10Å**		
	Id_{sat}	**ΔId_{sat}**	**L_{MET}**	**Id_{sat}[**	**ΔId_{sat}**	**L_{MET}**
RTP	0.546	—	22	0.900	—	30
LTP 1e20	0.541	-1%	34	0.918	2.0%	37
LTP 5e20	0.564	3.3%	34	0.977	8.6%	37
LTP 1e21	0.570	4.3%	34	0.988	9.8%	37

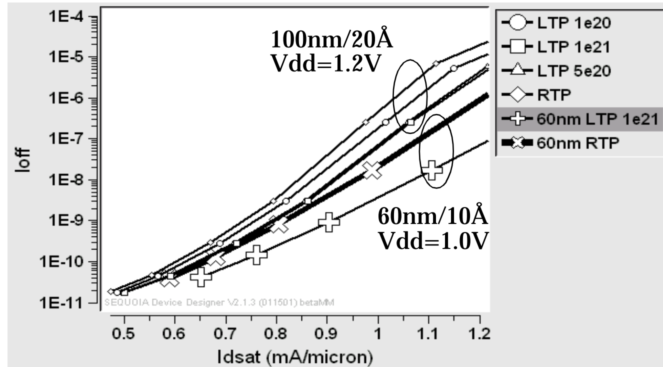

Fig. 11. NMOS universal curves for LTP and RTP SDE, Lpoly=100nm, the scaled 60nm device with Tox=10Å.

VII. Summary and Conclusions

Very deep-submicron transistor technologies with 100nm and below gate lengths will require significant improvements in Source/Drain extension profiles. Conventional RTP anneals cannot produce the necessary lateral profile steepness and peak concentration, thus significant losses in current drive capabilities can be caused by the residual source/drain resistance.

Laser Thermal Processing (LTP) dramatically improves both steepness and peak concentration of SDE profiles and reduces the source/drain resistance to insignificant levels for 100nm and below. Improvements in saturation currents of up to 10% and reduced short-channel effects can be expected for both NMOS and PMOS devices. However, continued oxide scaling below 20Å is necessary to fully realize these improvements.

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