Efficient Full-Chip Yield Analysis Methodology for OPC-Corrected VLSI Designs

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Abstract

Degradation of lithographic pattern fidelity is a major cause of yield loss in VLSI manufacturing. A general methodology for full-chip analysis and improvement of yield loss due to lithographic effects is proposed. The approach is based on: a) extraction of pattern fidelity statistics using a full-chip layout engine, b) full-chip Optical Proximity Correction (OPC) to improve pattern reproduction, and c) estimation of yield losses due to line variability, using transistor sensitivity to pattern registration obtained from physical transistor modeling. As a result, yield estimates related to either pattern reproduction fidelity or transistor parametric data variations (such as leakage or drive current) are generated. The method is efficient and well suited for application to modern VLSI designs of memory or logic devices.

Introduction

Within-chip variability of critical features such as poly lines due to limitations of manufacturing processes is a major cause of device variability and product yield loss. A significant fraction of this variability is a deterministic function of local layout patterns and properties of the manufacturing processes (lithography, etch, etc.).

In particular, optical proximity effects on the poly layer can degrade transistor parameters or even lead to catastrophic failures such as shorts or opens. Gate length variability is the main source of circuit-level variation and a major performance and yield limiter. Sensitivity of transistor performance to gate CD is a strong function of transistor architecture and, thus, the front-end manufacturing process. Reducing circuit-level variability can be achieved at two levels:

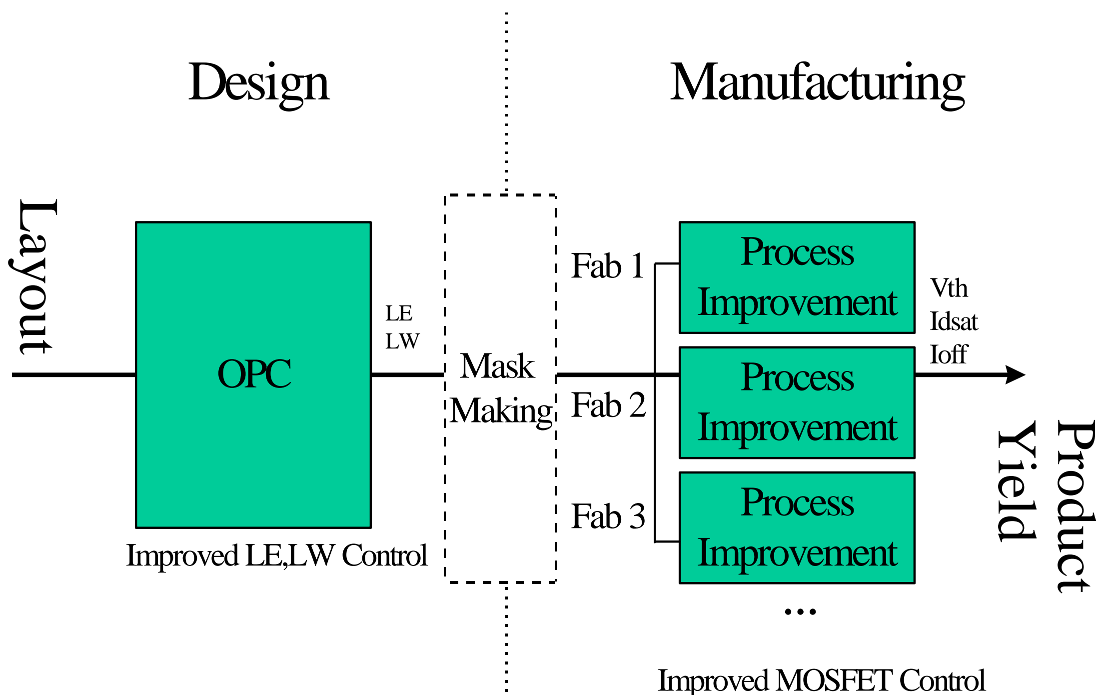


Fig. 1. Schematic representation of design phase and manufacturing phase yield optimization.

a) in the design phase, by applying Optical Proximity Correction (OPC) techniques to improve pattern reproduction.
b) in the process development or manufacturing phase of a product, by reducing sensitivity of active devices to pattern fidelity.

This work presents a comprehensive methodology aimed at predicting and optimizing product yield and performance by improving pattern control and reducing device sensitivity to the quality of pattern reproduction. Pattern variability is first statistically characterized at the full-chip level by Mentor Graphics Calibre OPC software. Its effects on device performance are then captured by SEQUOIA Design Systems' Device Designer software. Expected product yield and performance are extracted from the generated statistical distributions of transistor parameters. We demonstrate yield and performance improvements due to both enhancement of pattern fidelity by full-chip OPC and by de-sensitization of device parameters to pattern reproduction.

Separating Yield Components

The overall yield of can be calculated as a product of a random and a deterministic components:

$$Y_{total} = Y_{deterministic} \cdot Y_{random} \quad \text{(EQ 1)}$$

The deterministic component describes effects associated with pattern fidelity and the resulting circuit variability and performance degradation. The random component captures effects such as particle contamination. While a product's sensitivity to particle contamination is a function of the layout and, although random, will generally be different for different products manufactured in the same fab [1],[2], these issues are beyond the scope of this work.

The deterministic component can be further subdivided into catastrophic and parametric yield losses. Catastrophic yield loss occurs due to, e.g., shorts and opens. Parametric yield losses represent circuit failures due to transistor or interconnect parameters falling out of tolerable bounds, which are usually represented by spec limits.

$$Y_{deterministic} = Y_{catastrophic} \cdot Y_{parametric} \quad \text{(EQ 2)}$$

Since pattern fidelity degradation is the cause of deterministic yield loss, a lithography-related yield has been suggested as an estimate in [3] and extended for full-chip applications in [4]:

$$Y_{FullChipLitho} = \frac{\text{full chip count of CD within spec}}{\text{full chip count of all CD}} \quad \text{(EQ 3)}$$

The proper choice of spec limits will, in general, depend on the product and its performance targets. In particular, parametric yield loss will depend substantially on transistor and circuit architecture.

Line-End Variability and Catastrophic Yield Loss

Given the extremely large number of individual pattern elements in modern VLSI designs, statistical techniques must be used to capture pattern information in a form usable for further analysis. Below, we use two measures of pattern fidelity: variation of line-end and variation of line-width.

Line-end registration is an important criterion for pattern fidelity since excessive line-end shortening can cause MOSFET failures, as illustrated in Fig. 2. Line-end reduction of poly over active can lead to transistor short channel effects (threshold voltage variations, low punch through, and high leakage).

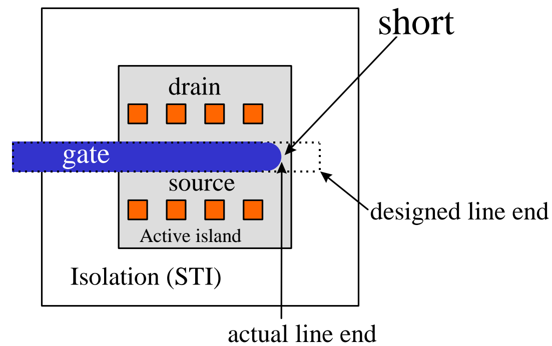


Fig. 2. Line-end rounding and shortening can lead to catastrophic failure.

A distribution of line-end placement errors extracted for a Mentor Graphics' test chip (containing line patterns drawn at 0.25µm design rules in various configurations and pitches) is shown in Fig. 3, left. Significant shortening of lines up to 130nm due to optical proximity effects is clearly visible. If uncorrected, they would lead to catastrophic failures of the type indicated in Fig. 2 (i.e. short-channel effects and possibly shorts).:

TABLE 1. **Line-end lithographic yield as a function of spec limit.**

Allowed line-end reduction	Yield before OPC	Yield after OPC
12.5nm	1.0%	97.7%
25nm	5.5%	99.9%
50nm	28.8%	99.9%

In order to prevent line-end shortening, full-chip automated OPC was applied to the test chip. By adding hammerhead serifs to the ends of poly lines, it was possible to

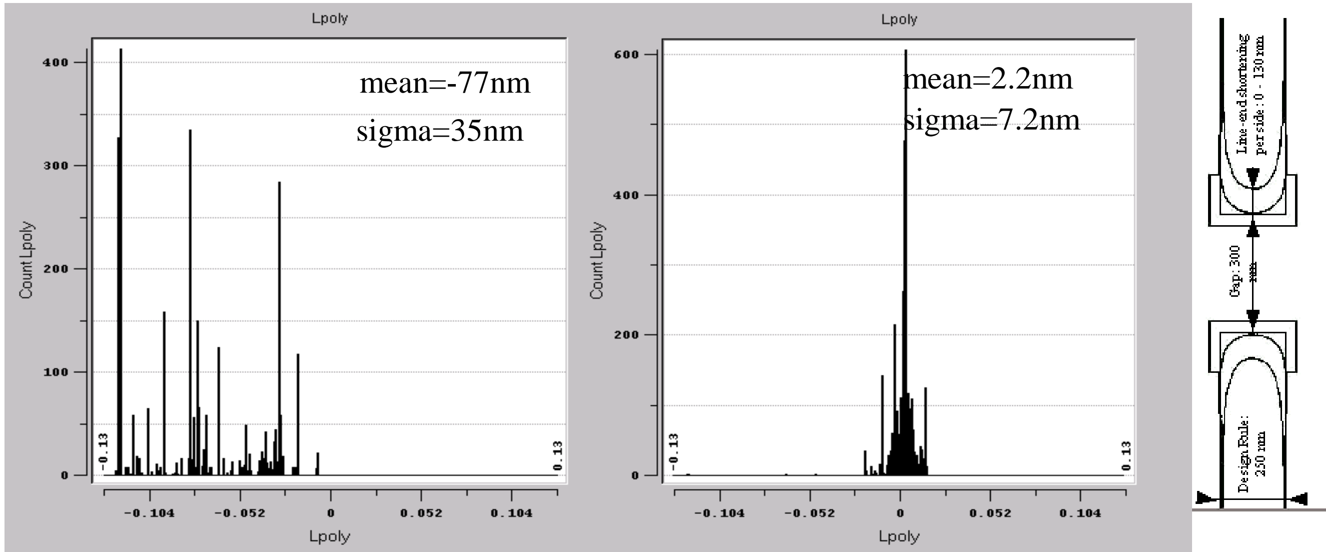
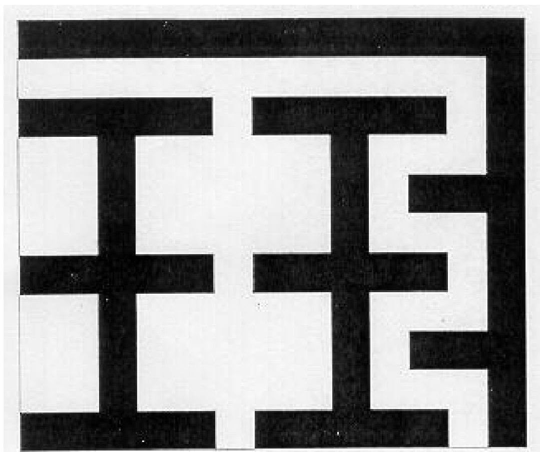


Fig. 3. Left: Distribution of line-end placement errors for a Mentor Graphics' test chip (0.25um design rules). Errors are defined as the distance between the actual and designed line-end locations. Right: Line-end placement errors after OPC for the test chip using the corrective hammerhead structure (far right).

dramatically reduce both the mean value and the variation of poly line end reduction, respectively from 77 to 2.2 nm and from 35 to 7.2 nm (Fig. 3, right). It is significant that after correction, the distribution became much closer to one of a Gaussian type, indicating that the first order problem has been solved by OPC and the residual error is random.

Given a specification limit for line-end placement errors, the lithographic yield can be estimated using (EQ 3) as shown in Table 1. The actual limit value depends on the process technology and the design safety marginFig. 4 and Fig. 5 illustrate layout modifications introduced by OPC and the resulting pattern changes [4].



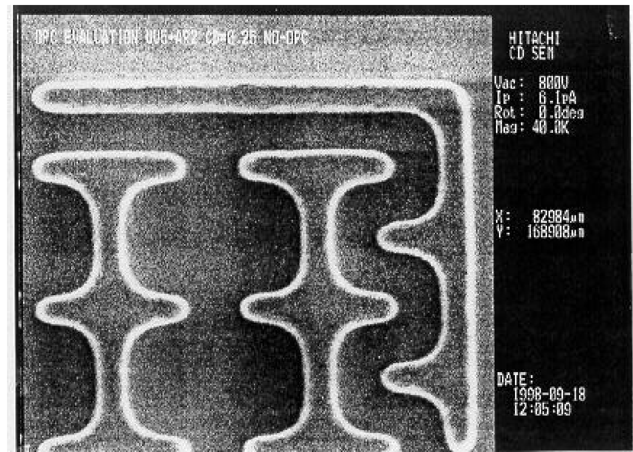


Fig. 4. left: Initial design (layout before OPC) and right: corresponding SEM on a wafer (after poly etch) [4].

Linewidth Variability and Parametric Yield Loss

Poly linewidth variability (called critical dimension or CD variation) determines circuit variability and, therefore, the yield and performance of the product. However, the mapping from linewidth to transistor parameters is nonlinear, which can produce highly detrimental non-normal distributions.

We used Mentor Graphics Calibre OPC software to extract the distribution of linewidth errors for the test chip. We then applied OPC and re-extracted linewidth errors.

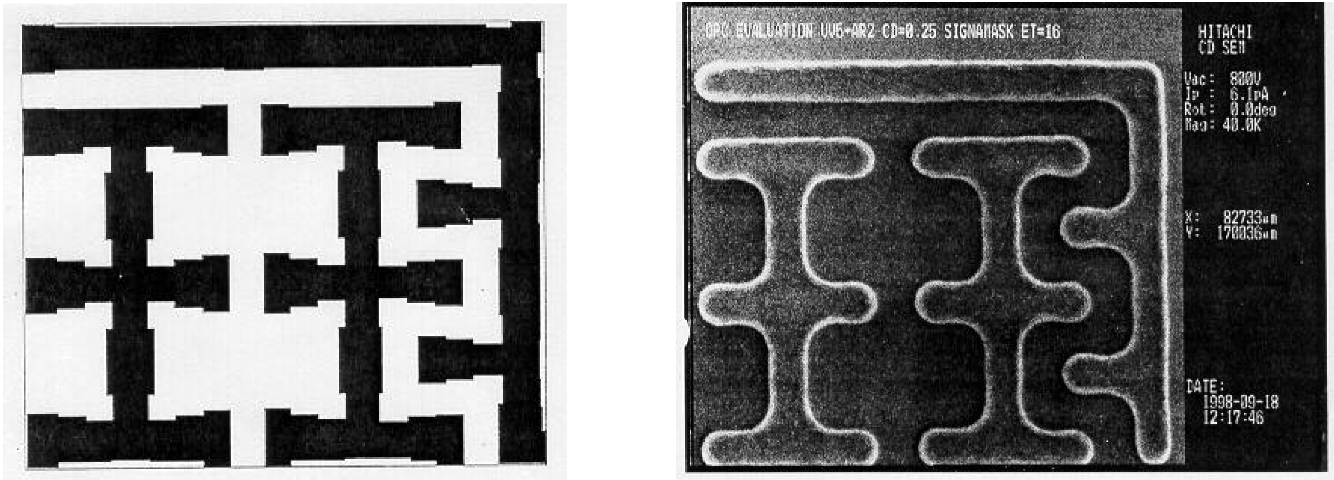


Fig. 5. left: Corrected design (layout after OPC) and right: corresponding SEM on a wafer (after poly etch) [4].

Results are shown in Fig. 6 (on the same scale as Fig. 3).

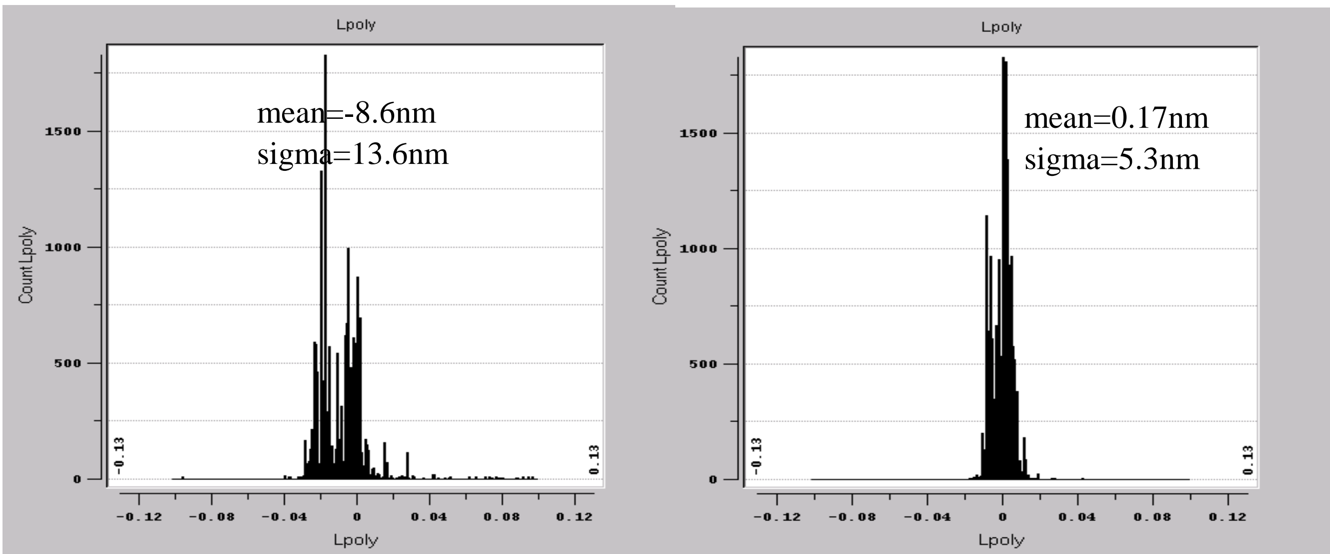


Fig. 6. Left: Linewidth errors before OPC. Right: Linewidth errors after OPC. The distribution has shifted and narrowed by 2.5X

As with line-ends, we see that OPC solves the systematic linewidth narrowing and reduces the standard deviation of the distribution by about 2.5X.

Transistor parameters were calculated using SEQUOIA Device Designer [5] for two hypothetical front-end processes, each optimized to produce the same saturation current at the target gate length of 0.25 microns. Compared to the baseline Process I, Process II has a more advanced architecture with a Halo implant (a common technique for 0.25µm technologies and below) added for better control of short-channel effects. Leakage current (Ioff) versus gate length (Lpoly) is shown in Fig. 7 for both processes. It is seen that Process II (squares) has a weaker Lpoly dependence, thus the same distribution of linewidths will result in a tighter distribution of Ioff than with Process I (circles).

With the calculated dependencies between Ioff and Lpoly, we can now re-state (EQ 3) in terms of transistor parameters that can be directly correlated with parametric and speed yield data. As an example, (EQ 4) shows a functional yield definition for a typical dynamic logic product. The speed yield can, in general, be described by a similar expression in terms of saturation current (low current generally means slower product):

$$Y_{parametric} = \frac{\text{number of MOSFETs with } Ioff < Ioffmax}{\text{total number of MOSFETs}} \quad \text{(EQ 4)}$$

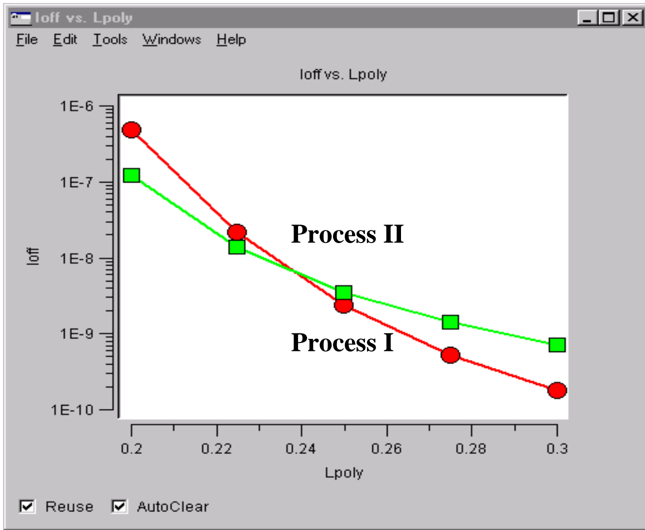


Fig. 7. Leakage currents Ioff (A/µm) versus Lpoly for two process technologies.

Distributions of Ioff are obtained by mapping linewidths data (Fig. 6) to leakage current using the curves in Fig. 7. With these distributions, we can estimate parametric yield improvements expected from OPC and/or process optimization. As an example, if circuit functional yield demands that a limit of 10 nA/um not be exceeded, we obtain the yield estimates shown in Table 2 and illustrated in Fig. 8.

TABLE 2. Functional yield estimates based on Ioff>10 nA/µm and line-width data.

	pre-OPC Yield	post OPC Yield
Process I	61.8%	100%
Process II	84.6%, Fig. 8 left	100%, Fig. 8 right

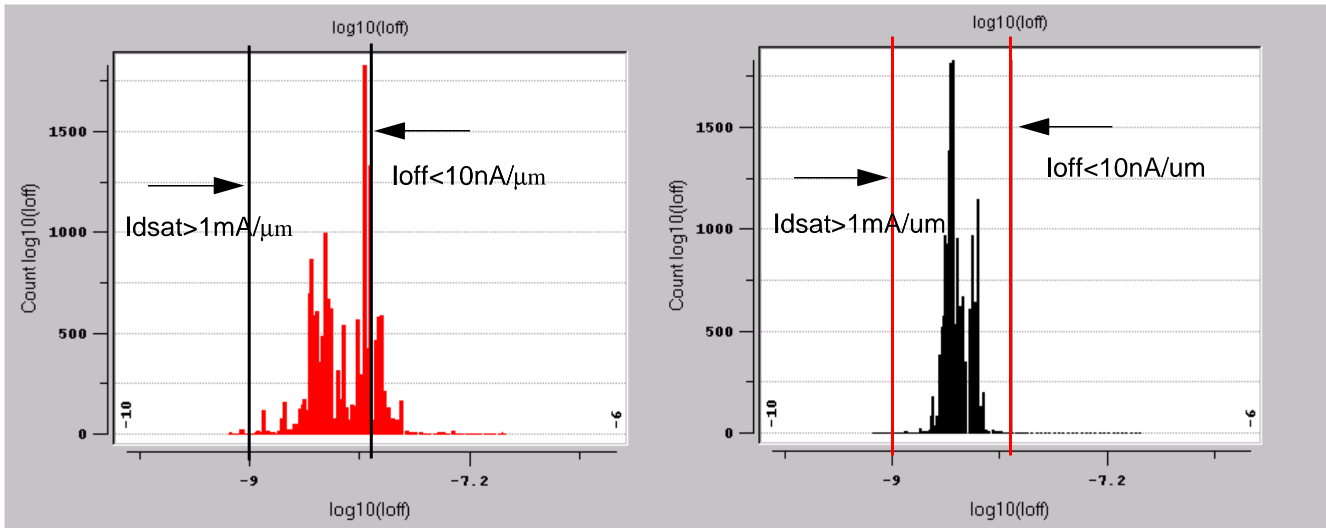


Fig. 8. Left: Leakage current distribution calculated for the test chip before OPC (Process II, 84.6% estimated parametric yield).
Right: Leakage current distribution calculated for the test chip after OPC (Process II, 100% estimated parametric yield).

For speed yield calculation, a lower limit for the drive current must also be considered in an expression similar to (EQ 4). Using 1mA/µm as an example for a lower Idsat limit, we obtain the window in Fig. 8 and yield estimates in Table 2 (Ioff and Idsat are strongly correlated for a given process technology. A lower Idsat limit therefore results in an equivalent lower Ioff limit).

In addition to yield improvement, the combined effect of improved CD control due to OPC and reduced device sensitivity due to process improvement (Process II) in our example offers the possibility of performance improvement. The distribution of transistor parameters shown in Fig. 8, right is rather narrow in comparison to the original window defined by $Ioff_{max}$ and $Idsat_{min}$. Consequently, the process can be retargeted towards higher Idsat (i.e. higher performance) without incurring any yield losses as shown schematically in Fig. 9. In other words, reducing the tail of the Ioff distribution makes it possible to shift the entire current distribution towards higher values to improve the speed.

Summary

A general methodology and a tool set for analyzing and optimizing full-chip catastrophic and parametric determin-

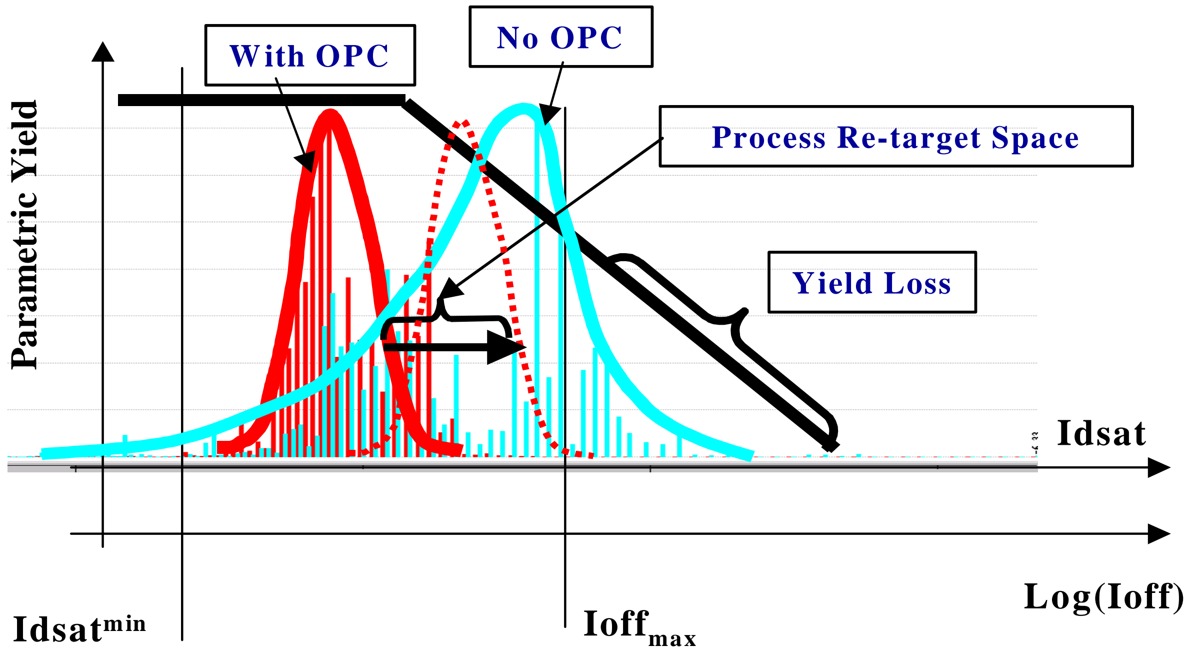


Fig. 9. Retargeting the process taking advantage of reduced device variability due to OPC or process improvement.

istic yield losses related to pattern fidelity has been presented. Line-end shortening, a potential cause for catastrophic faults (shorts), is dramatically reduced by Optical Proximity Correction (OPC). Line-width variability, a major source of circuit variation and parametric yield losses, is studied in conjunction with transistor-specific device sensitivity to line-width variation. Parametric yield and performance improvement can be addressed either in the design phase by OPC or during mass production by process optimization to reduce transistor sensitivity to pattern fidelity. The methodology can be used to aid strategic management decisions such as choosing an appropriate technology (or fab) for a product.

References

[1] C. H. Stapper, F.M. Armstrong, and K. Saji, "Integrated Circuit Yield Statistics," Proc. IEEE 71(4), April 1983

[2] W. Maly, A.J. Strojwas, and S.W. Director, "VLSI Yield Prediction and Estimation: a Unified Framework," IEEE Trans. CAD, CAD-5 (1), pp. 114-130 (1986)

[3] C. Mack, "Yield Modeling for Photolithography," Proc. of the Interface' 94 Conf., pp. 171-182, (1994)

[4] F.M. Schellenberg, V. Boksha, N. Cobb, J.C. Lai, C.H. Chen, C. Mack, "Impact of Mask Errors on Full Chip Error Budgets," SPIE Microlithography, March 1999

[5] SEQUOIA Device Designer User's Manual, SEQUOIA Design Systems, 1999