Circuit-Device Codesign for High Performance Mixed-Signal Technologies

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Abstract

System on Chip designs require low cost integration of analog and digital blocks. Often, the analog requirements are not considered sufficiently early in the device design cycle, resulting in devices that are suboptimal for the analog components. This paper presents an innovative methodology for deriving comprehensive device specifications based upon a set of Figure-of-Merit circuits which account for both analog and digital requirements. By utilizing these specifications for device design, a more efficient codevelopment of mixed-signal processes, libraries and products is possible. The methodology is illustrated with an example based upon an advanced 120nm CMOS technology.

Introduction

Low cost integration of baseband and RF analog functions with high performance logic is mandatory for System on Chip (SoC) applications [1]. Two deep-submicron technology (DSM) trends add to the difficulty of such integration. First, voltage scaling and tighter noise specifications increase the challenge of designing the analog IP blocks. Second, CMOS device optimization is typically driven by specifications that focus on increasing drive (I_{dsat}) and reducing off-state current (I_{off}), while minimizing junction and overlap capacitances. Analog device characteristics, such as g_m, g_{ds}, noise, matching, are often either ignored or deferred to subsequent refinement steps. Poor analog characteristics result in either suboptimal performances or expensive redesign of the analog blocks.

This paper describes a novel methodology for deriving a set of transistor design specifications based upon performances of a library of Figure-of-Merit (FOM) circuits. These specifications form the basis for obtaining device structures required to achieve transistor characteristics optimal for both analog and digital design. Transistor optimization for both analog and digital requirements improves the performance of the analog blocks while maintaining digital circuit speed. This methodology is demonstrated with an example of improving the analog performance of an advanced 120nm CMOS logic technology.

Codesign Methodology

Our methodology (Fig. 1) begins with a set of FOM circuits chosen to estimate the performance of a technology on a set of target applications. Transistor SPICE models for an existing technology are used as the starting point for optimization. These models can be obtained from either a previous technology or from a current technology targeted for optimization. The space of device characteristics is searched by parametrizing the SPICE models and optimizing for the value of the model parameters that result in the desired performance of the FOM circuits. The optimized model parameters are used to derive the target device characteristics.

Target devices are designed by using inverse modeling. The initial device characteristics are inverse modeled to generate structures which serve as an initial guess for deriving the optimized device structures. A direct comparison between the initial and final device structures provides the information necessary for the process modifications required to fabricate the optimized devices.

A. Model Parameterization and Optimization

The purpose of SPICE model parametrization is to create a space of device characteristics from which device designs that meet circuit requirements may be determined. At the same time, it is fundamental to maintain proper correlated relationship between model parameters necessary for feasible devices. To do this, first a set of constraints are included in device optimization to prevent exploring the infeasible region. Second, key SPICE model parameters are allowed to vary independently and a measure of distance from the initial device is used as an indicator of device feasibility; devices with parameter values close to the initial device are preferred over those with larger distance. For the application reported in this paper, 26 BSIM3v3 parameters are allowed to vary independently by up to 30% during optimization.

B. Device Design by Inverse Modeling

Inverse modeling techniques extract structure and doping information about a semiconductor device from its measured electrical behavior [2]. Since electrical measurements are readily available, inverse modeling is a very effective technique for structural characterization of DSM technologies where direct physical measurements are extremely expensive, inaccurate, and time consuming. We solve the problem of uniqueness associated with inverse modeling by utilizing a large number of device measurements: DC IV curves at different back biases (I_{dsat}-Vg, I_{dlin}-Vg, Id-Vd) and AC performance parameters (Cjs, Cjd, Cgd, Cgs).

Application Example

The co-design methodology described here was applied to improve the analog characteristics of transistors from an advanced 120nm CMOS logic technology. Analog performances were monitored using operational transconductance amplifiers (OTAs), current mirrors and MOS switches. Digital performances were monitored using multiple fan-out ring oscillators. The objective of the optimization was to improve leakage and output conductance while maintaining speed (i.e. reduce I_{off} and g_{ds}, while maintaining t_{pd}). Table I compares both the device level and circuit level performances of the initial and optimized transistors. Note the 10-15% reduction in g_{ds} and the reduction of I_{off} to bring it within the typical 1nA/μm requirement. This was achieved by only a 3% increase in t_{pd}. Fig. 2 and 3 compare IdVd characteristics of the optimized and inverse-modeled devices. 2-D doping distributions obtained from the inverse modeling of both NMOS and PMOS devices are shown in Fig. 4a and 5a. It was found that the optimized device characteristics could be achieved by adjusting the pocket doping profile of both devices. The net effect of those changes was to make the pocket profile more retrograde in both cases (Fig. 4b and 5b). No other changes to the device structures were required. These results are consistent with [3], which showed that the potential barrier created by a pocket implant at the surface has a negative effect on the device output conductance.

Conclusions

We presented a new methodology for obtaining transistor specifications and device designs based upon the requirements of a set of FOM circuits. This methodology makes it possible to derive device structures that concurrently optimize both digital and analog circuit design requirements. The method was illustrated by using it to improve the analog performance of an advanced 120 nm CMOS technology originally targeted for digital applications.

Tables and Figures

References

[1] Dennis Buss, "Device Issues in the Integration of Analog/RF Functions in Deep Submicron Digital CMOS", IEDM Tech. Dig., 1999

[2] Zachary K. Lee, et al., "Two-dimensional Doping Profile Characterization of MOSFET's by Inverse Modeling Using I-V Characteristics in the Subthreshold Region", IEEE Trans. Electron Devices, vol. 46, pp. 1640-1649, Aug. 1999

[3] A. Chatterjee, et al., "Transistor Design Issues in Integrating Analog Functions with High Performance Digital CMOS", VLSI Tech. Symp. pp.147-148, 1999.

[4] SEQUOIA Device Designer User's Manual, SEQUOIA Design Systems, 1999

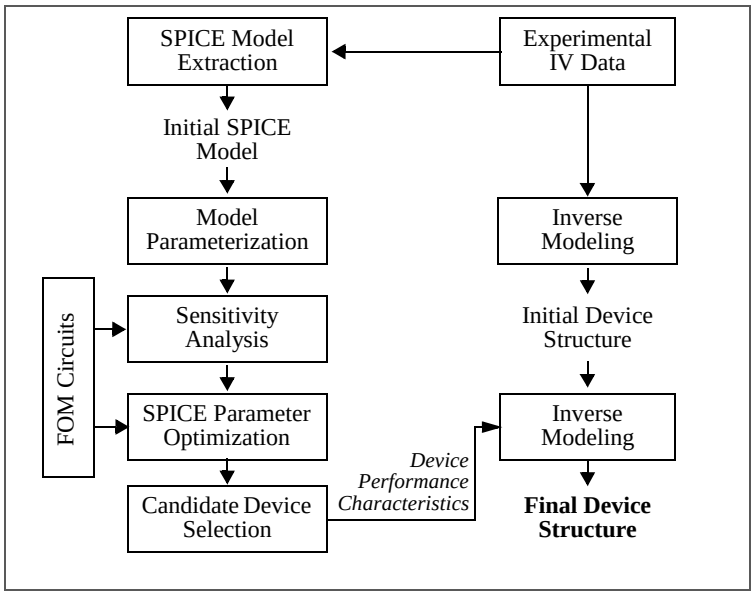

Fig. 1 Design flow for deriving device designs from FOM circuits

TABLE I : Optimized circuit/device performance

Circuit/ Device	Parameter	Initial	Optim.	%
NMOS	Vtsat (mV)	268	286	+7%
	Vtlin (mV)	400	397	-1%
	Idsat (μA/μm)	692	673	-3%
	Ioff (nA/μm)	1.43	0.877	-40%
	gdsmin ($\mu\Omega^{-1}$)	88.6	7.86	-11%
PMOS	Vtsat (mV)	215	250	+16%
	Vtlin (mV)	404	440	+9%
	Idsat (μA/μm)	340	327	-3%
	Ioff (nA/μm)	1.46	0.49	-66%
	gdsmin ($\mu\Omega^{-1}$)	96.3	82.6	-15%
Ring Osc.	tpd (psec)	16.7	17.3	+3%
OTA (p-load)	Av (dB)	35.7	33.4	-7%
	f3db (kHz)	363	474	+30%
	Pwr (μW)	1.19	1.13	-5%
OTA (n-load)	Av (dB)	33.7	33.13	-2%
	f3db (kHz)	254.5	269.5	+6%
	Pwr (μW)	1.22	1.22	0%

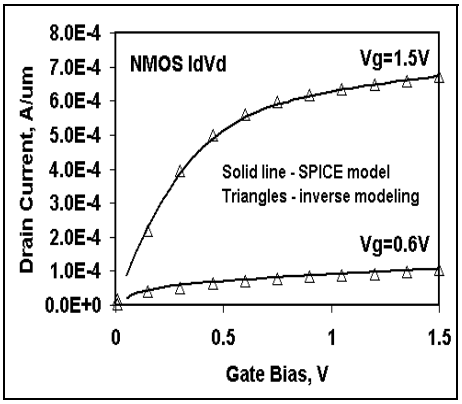

Fig 2: Drain curves of the optimized NMOS

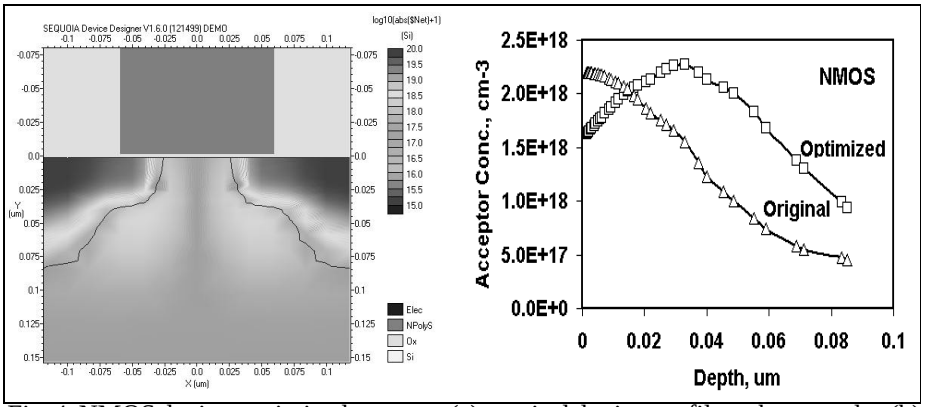

Fig. 4: NMOS device: optimized structure (a), vertical doping profile at the gate edge (b)

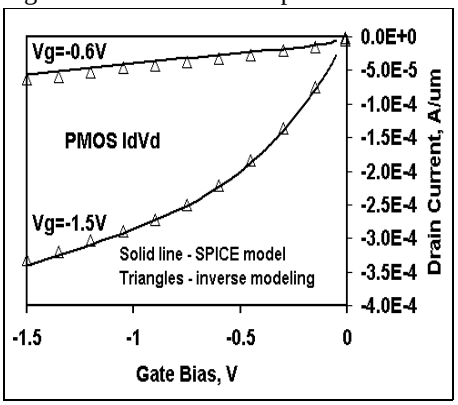

Fig 3: Drain curves of the optimized PMOS

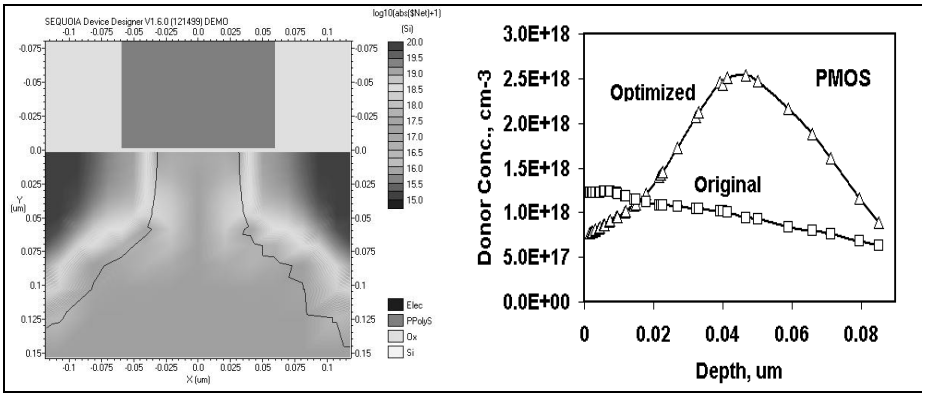

Fig. 5: PMOS device: optimized structure (a), vertical doping profile at the gate edge (b)