Investigations of Salicided and Salicide-Blocked MOSFETs for ESD Including ESD Simulation.

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Abstract

Standard salicided MOSFETs have been repeatedly shown to have inferior ESD protection properties in comparison to salicide-blocked MOSFETs. Standard explanations typically attribute this to shallower current flow and higher peak current density in salicided devices due to the higher conductivity of salicides. In this work we present a numerical analysis of the phenomenon using physical mixed-mode circuit-device simulation. Our results show that the inherent lack of thickness uniformity known to exist in salicide layers can lead to local concentration of current flow and thus local failure of the device.

1. Introduction

Many authors have discussed the merits of using salicide-blocked grounded gate MOSFETs as primary protection elements in I/O circuits [1]-[3]. The usual explanation (offered with a great deal of handwaving) is that the blocked salicide device allows current to flow deeper into the silicon during an ESD event, thereby dispersing heat more effectively, in turn leading to better ESD performance [4]-[5]. For salicided transistors, the current flow is restricted closer to the surface (where the salicide resistance is low), leading to higher temperatures and lower failure voltages compared to salicide-blocked devices [6]-[7].

Our investigations show that the above picture is misleading and does not represent the major effect. We show here that the major improvement of salicide-blocked devices comes from a more uniform turn-on of each grounded gate NMOS finger in a multi-fingered structure (many devices in parallel). Due to salicide thickness variation in salicided MOSFETs, the performance of each finger can be different, leading to non-uniform current density in the fingers which can lead to catastrophic failure of the finger with the thickest salicide. For salicide-blocked devices, a more uniform finger turn-on is more likely.

The interpretation of this result is owing largely to a novel simulation software [8] which we use for characterizing an ESD event. In comparison to other device simulation tools (PISCES, Medici, etc.) the main differences are:

1) It does not require a process simulator to generate the input device structure. One can inverse model a transistor's profiles from desired electrical characteristics that are specified by the user (Vth's, Idsat, breakdown voltage, etc.).
2) Manual gridding is not required. The simulator constructs an efficient grid without user intervention.
3) An I/O circuit with multiple elements (mosfets, resistors, diodes, etc.) can be entered using built-in schematic capture and simulated without exhausting the grid node count limit of more traditional device simulators.

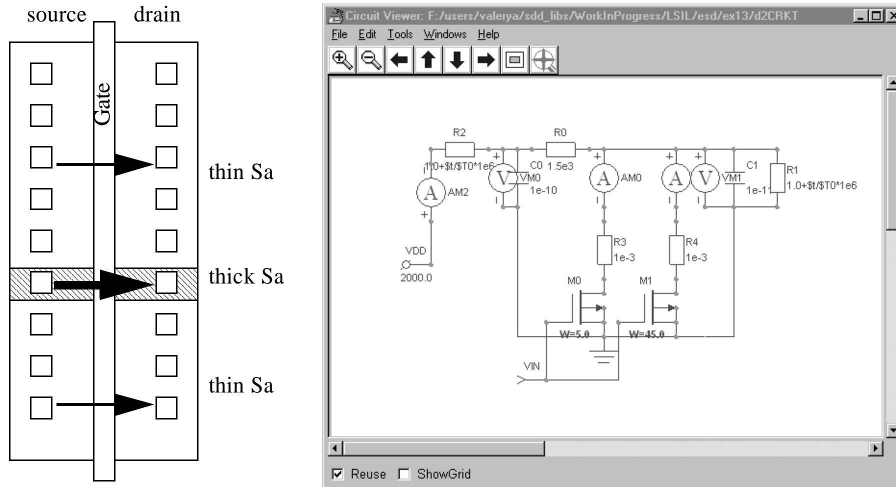

Fig. 1. Simplified view of the ESD protection MOSFET and the simulated circuit: to model salicide thickness variation, two grounded MOS slices (fingers) in parallel with different salicide thicknesses are used. The total device width is 50µm. Thin salicide fingers account for 45µm (M1), the remaining 5µm are modeled as a thick salicide MOSFET finger M0.

And finally, compared to ESD simulators based on Spice-like circuit simulation [9]-[10], a device simulator is capable of dealing with geometry and doping variables (such as salicide thickness) which a circuit simulator cannot do.

2. Mixed-Level ESD Analysis

In Fig. 1, we show the circuit used to simulate an HBM event. The protection device consists of a grounded gate MOSFET comprised of two parallel MOSFETs, a thin salicide one with a width of 45µm and a thick salicide one with a width of 5µm.

Fig. 2 (left) shows a cross section of the MOSFET indicating the salicide thickness parameter. MOSFET doping profiles were specified according to SIMS measurements. Simulated breakdown curves (Fig. 2, right) demonstrate good agreement with measured data without any additional calibration. The differences between the two before breakdown are insignificant. After breakdown, however, the thin salicide device has a higher on resistance, once again showing that salicide thickness variation will lead to variation in finger performance.

Fig. 3 shows plots of electric potential along a horizontal cross-section under the salicided drain of the two MOSFETs. Higher voltage drop and therefore higher on-resistance are evident for the thin-salicide case (crosses). Since all transistor slices (fingers) are connected in parallel, lower on-resistance of a slice results in higher dissipated power and stronger heating there.

In Fig. 4 (left), we show the current density per micron of MOSFET width through the two parallel protection GGNMOSs, and in Fig. 4, right we show the output voltage VM1 as well as peak temperatures for the two devices. The thicker salicide device (5µm width) has higher current density leading to a higher temperature in this device. Note that this is the effect we expect based on standard thinking but for the wrong reason. The standard claim is that the thicker salicide device should heat up more because

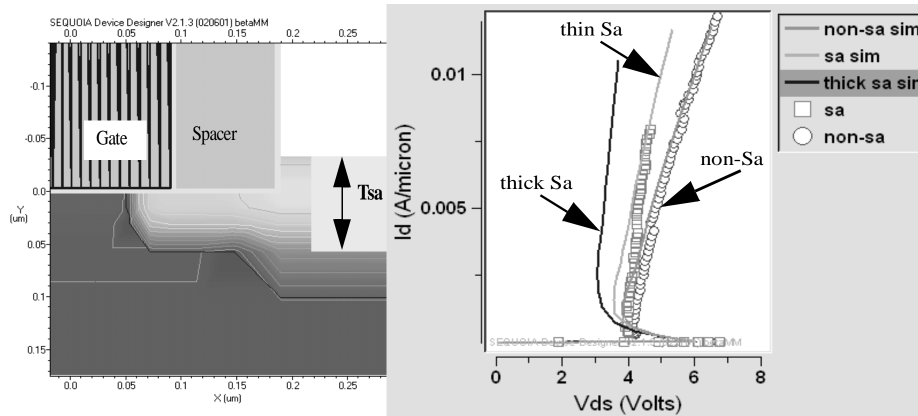

Fig. 2. Left: Parametrized MOSFET with the salicide thickness parameter Tsa indicated (thick salicide case is shown). Right: measured (symbols) and simulated (lines) breakdown curves for the non-salicided, thick- and thin-salicide devices with Lpoly=0.18μm. Good agreement between simulation and experimental data is observed. Salicide thickness has a significant effect on post-breakdown on-resistance.

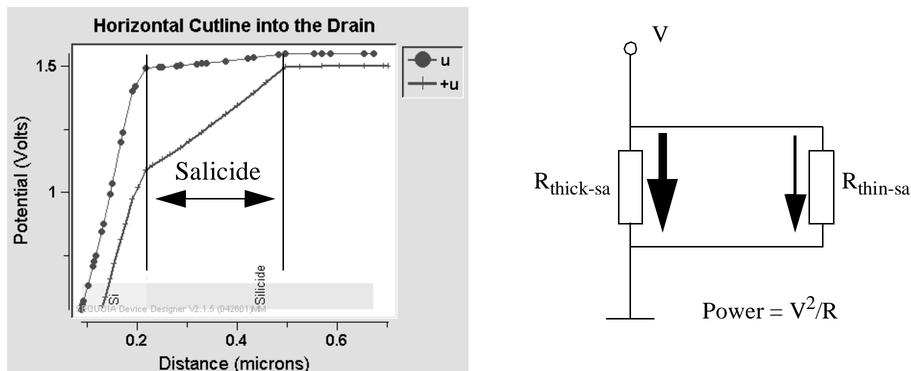

Fig. 3. Electric potential during the ESD pulse along a horizontal cutline close to the surface of the thick-sa MOS (circles) and thin-sa MOS (crosses). Much higher voltage drop in the salicide region for the thin-sa device is evident, indicating its higher on-resistance. Since all MOS slices (fingers) are connected in parallel, the slice with the lowest resistance pulls the highest power and therefore heats up the most. In our case it is the thick-sa device.

its current doesn't flow deep enough into the silicon to benefit from better heat dissipation of surrounding silicon. Here we see that it heats up more because it has lower resistance and draws more current. In addition, this clearly shows that salicide thickness variation can lead to large differences in current drawing and heating of the device.

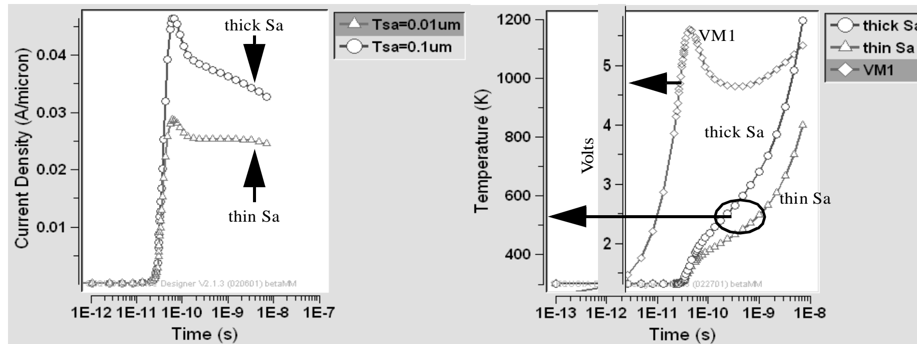

Fig. 4. Left: Current per unit width, the thicker salicide device pulls a higher current density and consequently heats up faster. Right: Output waveform VM1 (see Fig. 1, blue curve) and peak temperatures in the thick salicide device (red) and thin salicide device (green). Permanent device failure occurs between 800K (aluminum failure) and 1200K (silicon melts).

3. Conclusions

We demonstrated a novel approach to the analysis of ESD protection circuits. The approach is based on a mixed-level simulation system, which combines physical depth of analysis with complex circuit effects important for ESD events. The simulation system was applied to study salicided versus non-salicided grounded gate MOSFETs.

Our analysis suggests that the experimentally well-documented ESD-weakness of salicided MOSFETs is caused by the significant intrinsic variability of salicide layers. Locally varying salicide thickness can lead to locally reduced device on resistance, thus increased current density, local heating and possible local failure at the thick salicide locations in the device.

4. References

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