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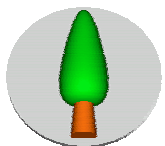


A Novel Design-Process Optimization Technique Based on Self-Consistent Electrical Performance Evaluation

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Overview

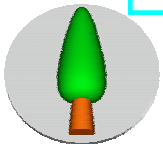
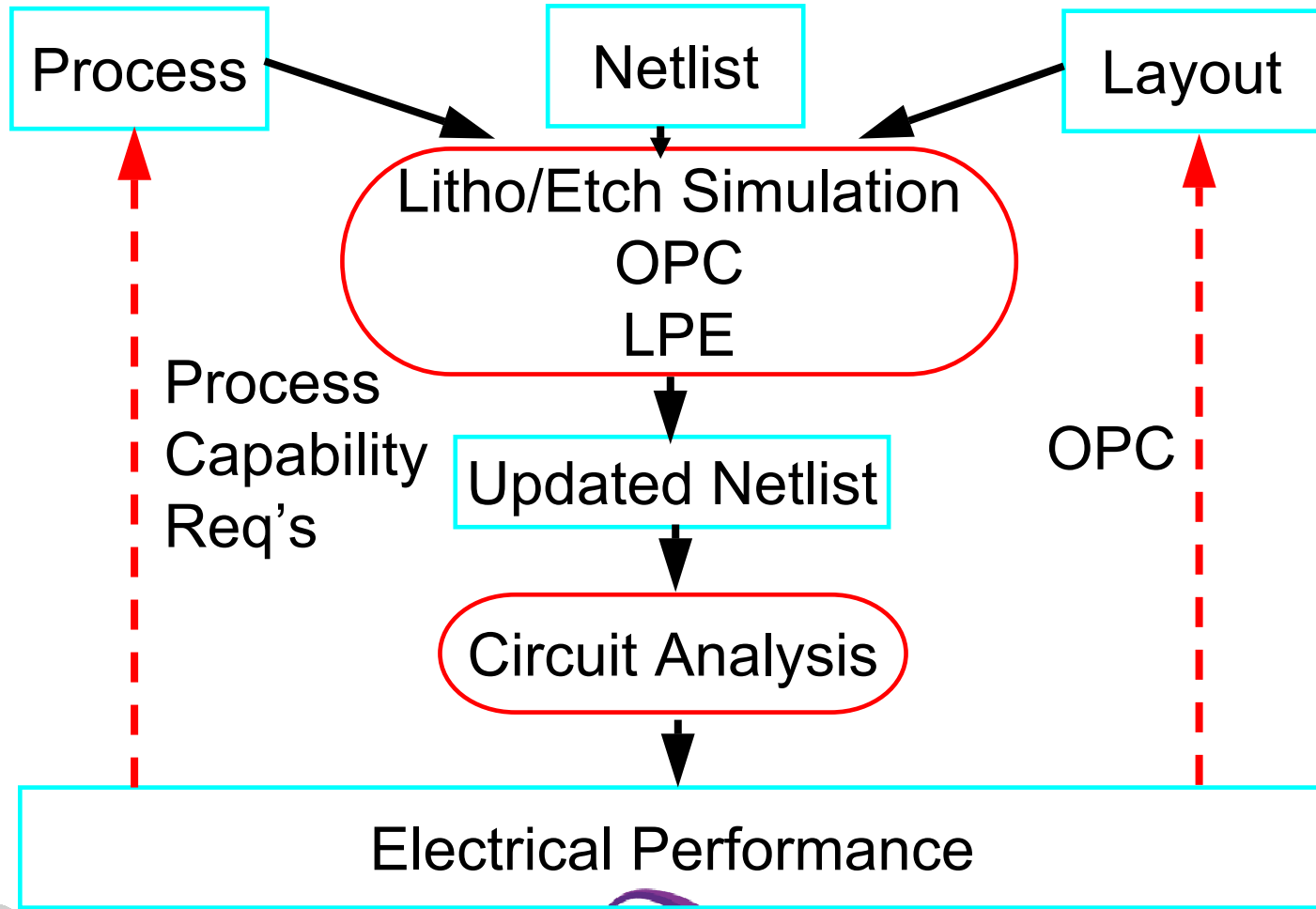
- Introduction
- Cell design choices: Design A, Design B
- Light source design: Vertical Dipole
- SNM Calculation
- Results
- Summary



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TrueDFM™ Flow



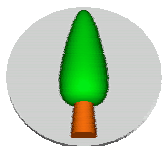
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SPANSION™



Applications of TrueDFM™

- Circuit performance-based manufacturability assessment of circuits manufactured in a specific process. Analysis of electrical performance, variability and process window
- Impact of FEOL and litho process changes/updates on circuit performance and yield
- Statistical sign-off verification of manufacturability (electrical DRC)

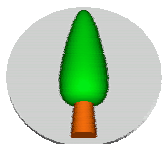


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This Work

- In this work we compare manufacturability of two different SRAM cell layout design options
- Manufacturability estimated using SNM (Static Noise Margin) versus defocus and exposure
- SNM calculated using process simulation (litho+etch) and subsequent SPICE simulation of the cell using BSIM3 transistor models
- Process windows are compared for the SRAM cell design options
- Light sources: an annular source and a vertically oriented dipole source

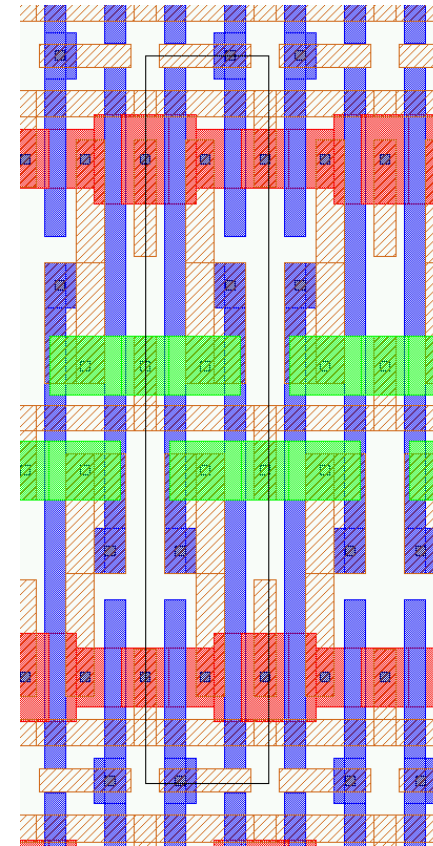
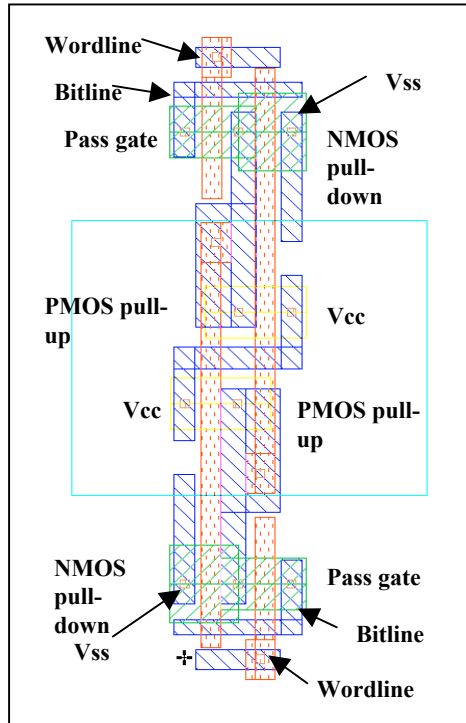


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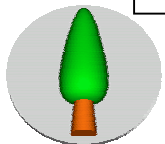


Cell Design Choices: Design A

Vertical orientation of inverter and pass gates



Cell Context

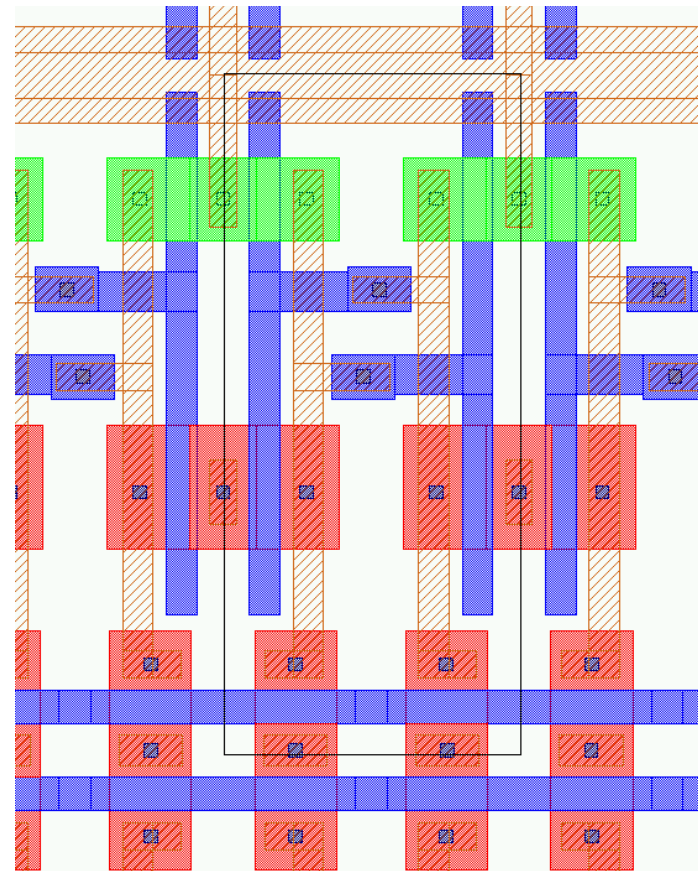


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Cell Design Choices: Design B

- Vertical orientation of inverter gates, horizontal orientation of pass gates
- Anisotropic cell layout results in potentially strong interaction with light source designs

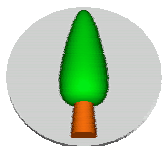
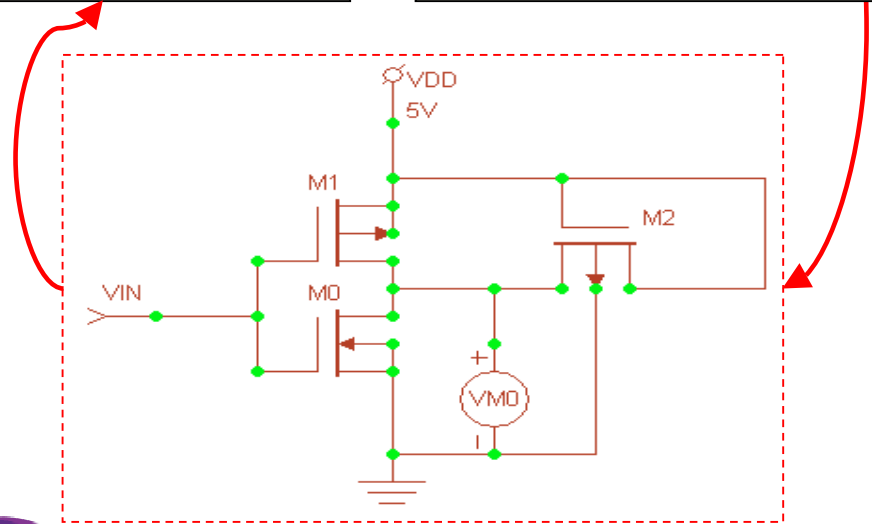
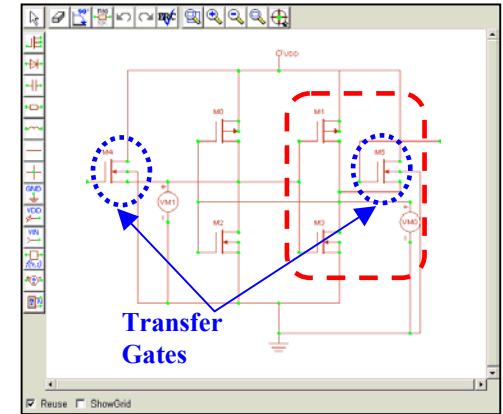
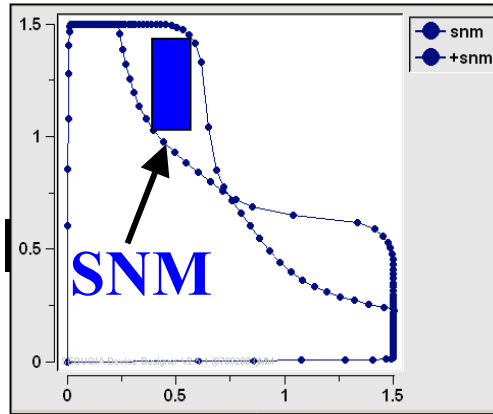


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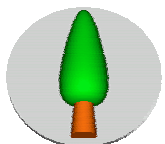
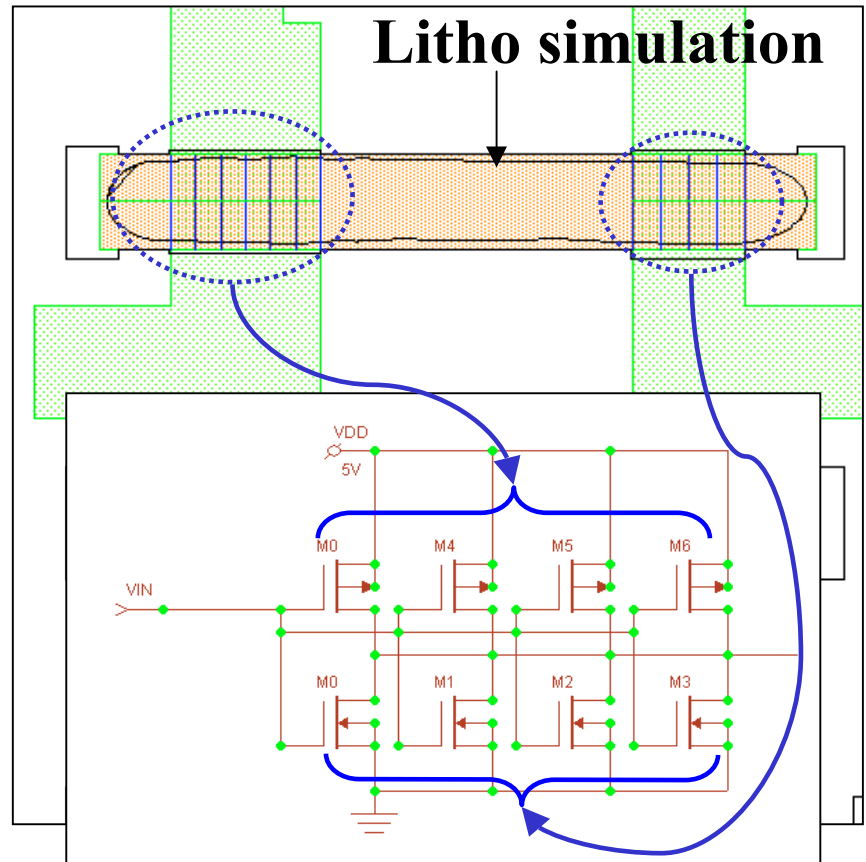
Electrical Analysis of SRAM Cells

- Transfer characteristics of inverters in the cell determine its operation stability
- Static Noise Margin extracted from butterfly plots
- SNM driven by beta ratio $M0/M2$



Modelling MOSFET Behaviour

- Channel length variation across a MOSFET is captured by a quasi-3D MOSFET model
- Each MOSFET is represented by a subcircuit with multiple MOSFETs in parallel
- Each slice-MOSFET has its own extracted L_{poly} and W

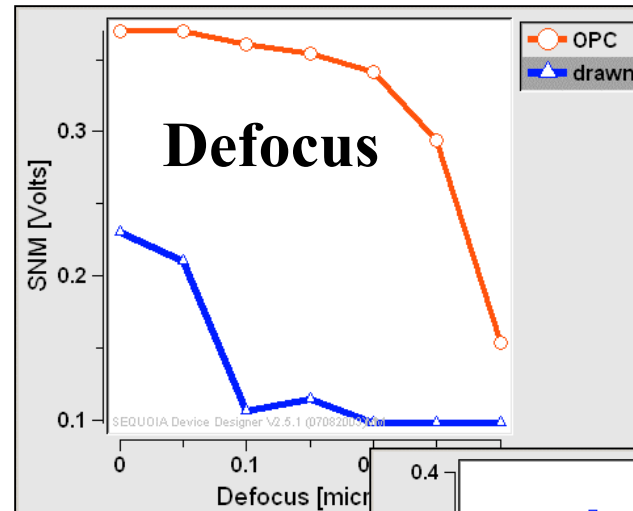


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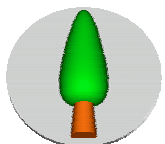
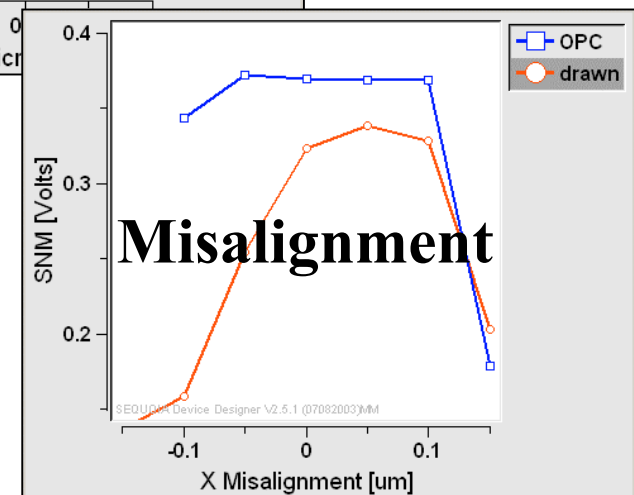


Electrical Process Window

- Electrical process window is calculated by extracting SNM for each setting
- Process windows for respective process conditions are evaluated
- Manufacturability of layout options is electrically quantified



Examples

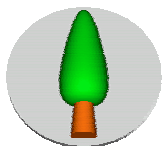
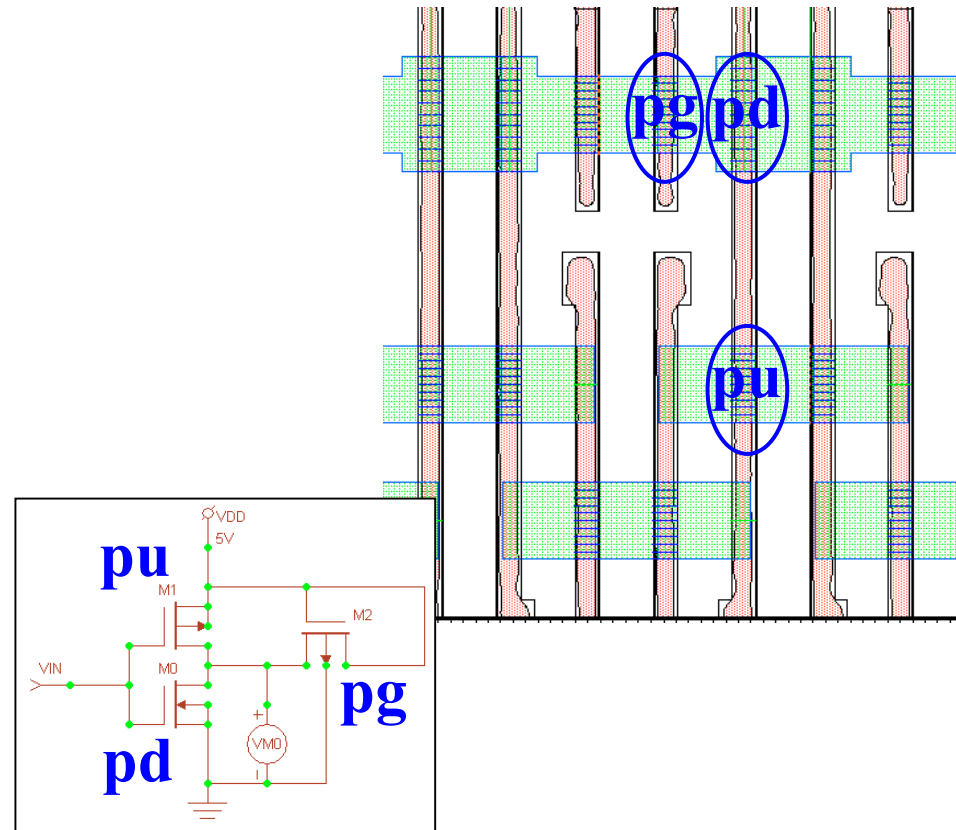


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Results: Design A

- At def=0.2um significant pattern distortion evident
- Lines tend to become narrower
- Line width not constant within MOSFET gate lengths
- PG and PD distortions are similar

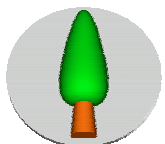
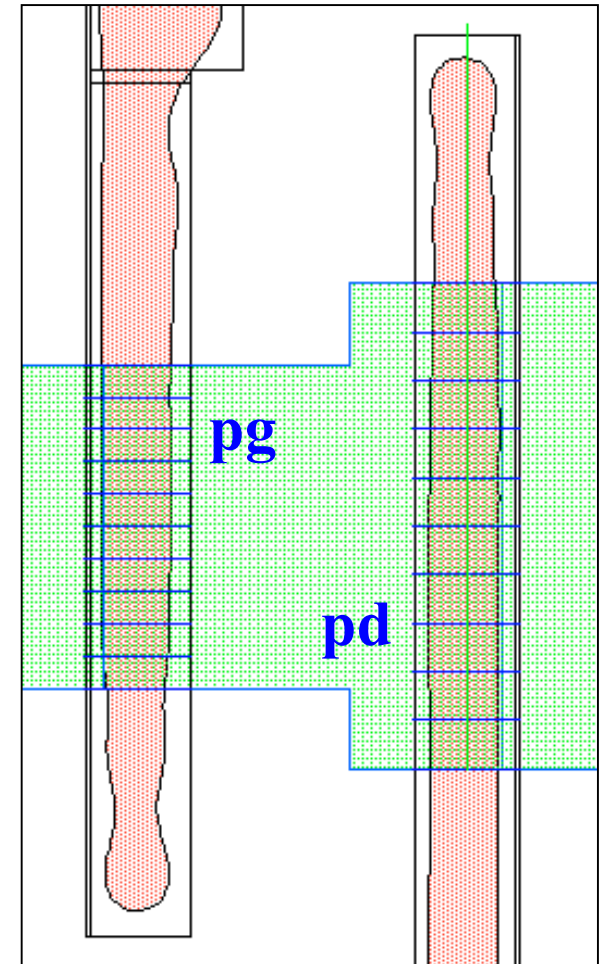
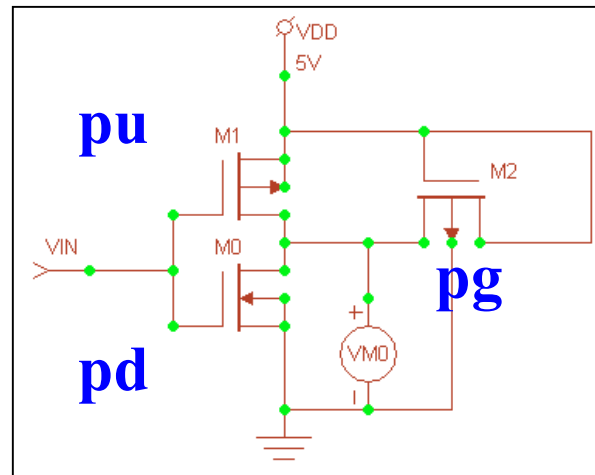


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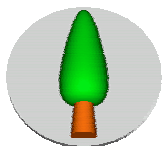
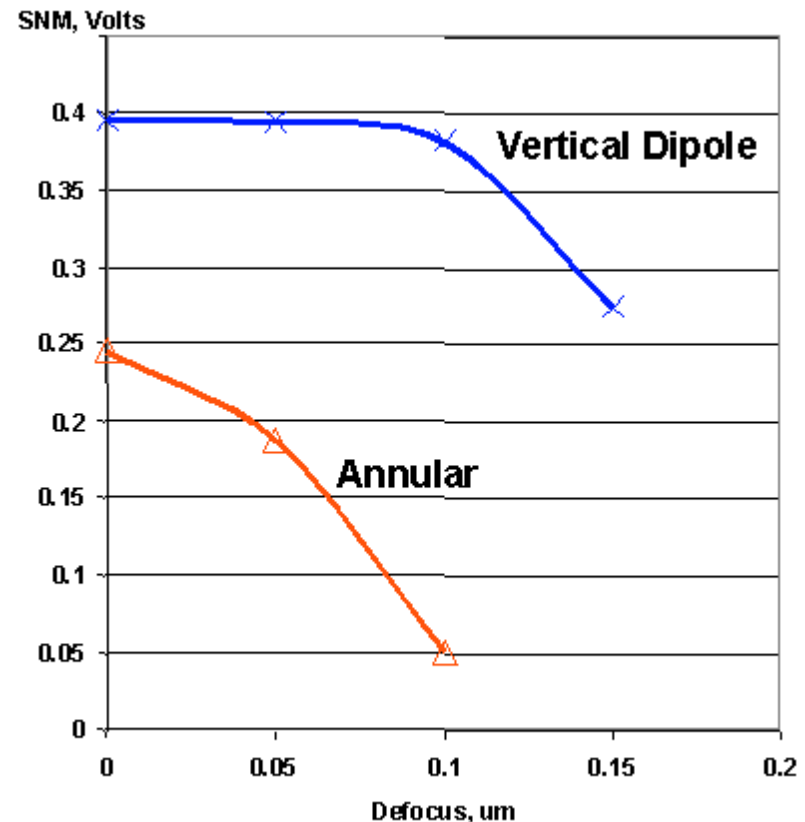
Results: Design A

- Passgate and pull-down MOSFETs print similarly
- SNM primarily driven by beta ratio PD/PG
- Impact of defocus on SNM is mitigated



Results: Design A SNM

- SNM calculated versus defocus for the two light sources
- Vertical dipole provides best performance and process window for this cell
- Annular light source degrades SNM
- Vertical lines print wide with dipole, SNM is high

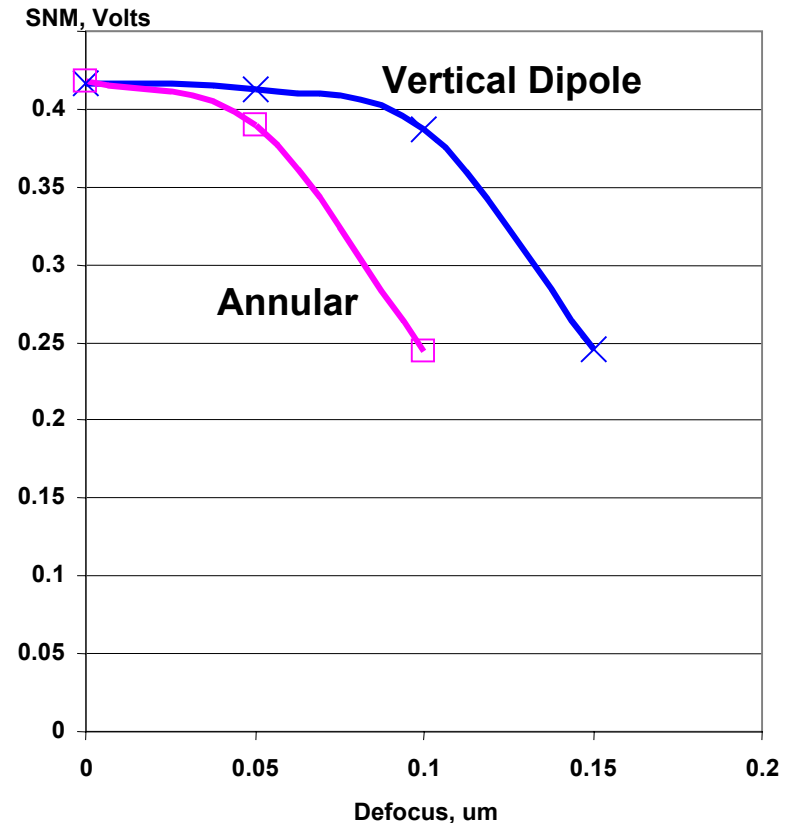


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Results: Design B SNM

- Design B cell characterized by vertical PD and horizontal PG FETs
- This cell is optimized for vertical dipole light source using layout pre-correction
- Vertical dipole light source has best performance and process window
- Annular light source is worse

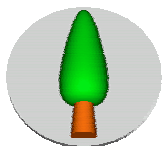
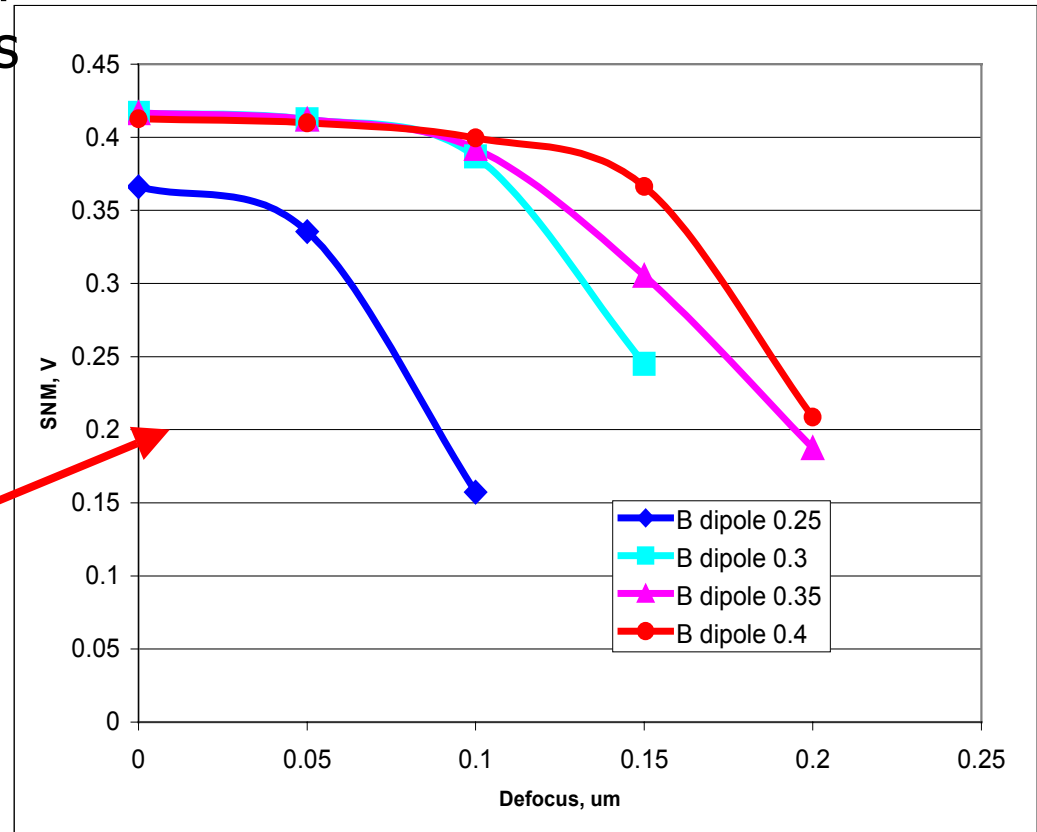
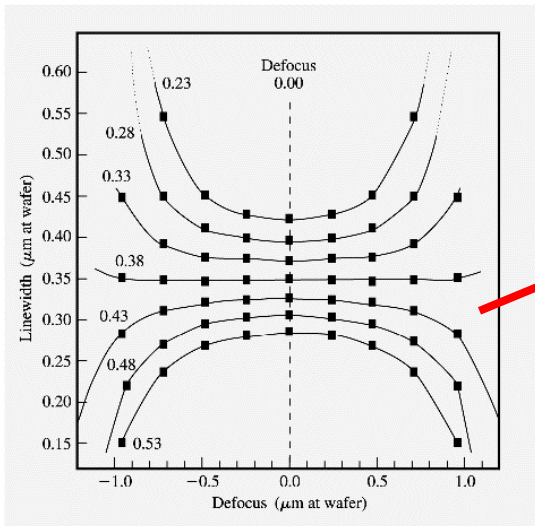


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SNM vs. Exposure, Defocus

- SNM versus defocus for a set of exposure levels
- Electrical equivalent of Bossung plot

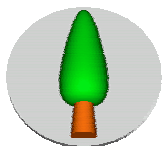


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Summary

- ⇒ As a result of layout pre-correction both cell designs options are manufacturable with dipole light source
- ⇒ SNM performance degrades for annular light source
- ⇒ Degradation for annular light sources is very strong for Design B, this cell is sensitive to light source type and likely more sensitive to aberrations



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