The Effects of Substrate Coupling on Triggering Uniformity and ESD Failure Threshold of Fully Silicided NMOS Transistors

Yoon J. Huh, Valery Axerad*, Jau-Wen Chen and Peter Bendix
Device Technology Gr., LSI Logic Corp., 1551 McCarthy Blvd. J-100 Milpitas CA 95035, (408) 954-3244
*Sequoia Design Systems, 137 Chapman Rd. Woodside, CA 94062, (650) 529 1704

Abstract

We present a multi-finger turn-on model incorporating substrate coupling effects in multi-finger NMOS transistors during ESD events. It is demonstrated that the substrate coupling enables uniform triggering in a multi-finger structure. In addition, we show that fully silicided transistors can be used successfully as an ESD protection device without any design/process options if the effective epi thickness is larger than 1.5µm or bulk wafer is used.

Introduction

To ensure electrostatic discharge (ESD) robustness of silicided transistors, numerous papers have analyzed the cause of low voltage ESD failure of silicided transistors and suggested solutions to overcome the silicidation effects [1]-[3]. All efforts to improve the ESD performance of silicided transistors are based on the standard thinking that V_{t2} (the voltage for triggering into second breakdown) should be greater than V_{t1} (the voltage at which snapback occurs) in order for all fingers in a multi-finger structure to turn on prior to failure. Our investigations show that the above standard thinking is misleading and does not represent the major effect due to ignoring substrate coupling effects in previous works. Based on our multi-finger turn-on model, we demonstrate that substrate coupling enables uniform triggering in multi-finger devices even with $V_{t2} < V_{t1}$. The impact of epi thickness (t_{epi}) on uniform triggering in multi-finger devices is also studied. ESD performance was evaluated from test structures and real products using 0.13µm and 0.18µm technologies. The interpretation of these results is owing largely to novel simulation software [4] which we use for characterizing ESD events.

Multi-Finger Turn-on Model for NMOS Transistors

Fig. 1 shows the cross section of a multi-finger structure for both bulk and epi wafers. Note that only two fingers are depicted in Fig. 1. To understand the triggering mechanism in this multi-finger structure, a novel mixed-mode ESD simulation was performed. The simulation structure for bulk wafers is shown in Fig. 1 (a). It is assumed that the left transistor has a 10% lower channel doping to consider process-induced non-uniformity. The source current is measured separately to monitor when each transistor triggers. Fig. 2 shows the current waveforms along with the drain voltage. The drain voltage drops by a volt from its peak right after the left finger triggers. It is interesting to note that the right finger triggers as well after a delay time of 1ns even at a lower drain voltage than its trigger voltage. This implies that the triggering of the second transistor doesn't rely on the drain voltage alone. Fig. 3 shows how potential contours spread out from the channel of the first finger and reach the second and third finger to trigger them. This result clearly shows that the uniform triggering of multi-finger structures is achieved by substrate coupling effect. The result for epi wafers is shown in Fig. 4. A t_{epi} of 0.75µm was used. Since p+ dopants in the p+ substrate move up to the p- epi layer, the effective p- epi thickness (t_{epi}) is reduced with heat cycle for a given process. The effective epi thickness is defined by the distance from the silicon surface to the p- epi with a dopant concentration of 1E18/cm^3 as shown in Fig. 1 (b). We observe that the left transistor with a lower channel doping absorbs the entire ESD current along with the substrate current (I_{sub}) since the neighboring NMOS (F2) doesn't trigger. This result is not consistent with the bulk wafer result that neighboring fingers are turned on by substrate coupling effects. The potential contour shown in Fig. 5 confirms that substrate coupling is not sufficient for uniform triggering in this case. The impact of t_{epi} on substrate-coupling-induced multi-finger triggering is shown in Fig. 6. Three fingers of NMOS were used in this simulation. We see that triggering uniformity in multi-finger structures is a strong function of t_{epi}. In particular, the delay time for triggering between fingers varies with t_{epi}, which determines current distribution among the fingers. Note that the third finger (F3) shows a larger delay time than that of the second finger since it triggers after the second finger.

Fig. 7 represents a multi-finger turn-on model incorporating substrate coupling effects. For epi-type substrates the heavily doped bulk can be considered as one electrical node and only the resistance of the p- epi layer has to be considered as spreading resistance. As indicated in the potential contours of Fig. 5, the substrate potential floats up under the left gate but cannot spread laterally to raise the potential under the second poly finger. Because of the low resistivity and thickness of the p+ bulk, the injected hole current flows almost directly down through the p- epi layer into the p+ bulk. Therefore, the model equation for the case of weak finger to finger substrate coupling (poor triggering uniformity) may be written as

$$\mathbf{G_{vertical} > G_{lateral}} \qquad \textbf{(1)}$$

The parameters $G_{vertical}$ and $G_{lateral}$ represent the conductivity of the vertical (finger to p+ bulk) and lateral (finger to finger) direction, respectively. For the bulk wafer and epi-type substrate with t_{epi} larger than 1.5um cases, we would expect that the multi-finger triggering occurs with

$$\mathbf{G_{vertical} < G_{lateral}} \qquad \textbf{(2)}$$

In Fig. 7, increasing the source resistance (Rs) improves the coupling effects since Rs*Is1 enhances the propagation of the substrate potential (Φ1) to the neighboring finger (Φ2). This phenomenon can be understood by comparing the source current of the right finger in Fig. 1 (b) with different Rs values as shown in Fig. 8. The same reasoning can also be applied to non-silicided (silicide blocked) transistors that have higher Rs than that of fully silicided transistors.

Experimental Results for Fully Silicided Transistors

Fig. 9 shows the width dependence of fully silicided multi-finger structures for a 0.18µm technology using bulk wafers. As expected from our multi-finger turn-on model, the failure current (i_{t2}) shows a strong width dependence like non-silicided transistors. We have used fully silicided NMOS transistors as a primary protection device and/or self-protecting output drivers in real products without any design/process options, and pass 3000V HBM and 700V CDM. A high current I-V curve measured from a real IO of our 0.13µm technology is shown in Fig. 10. These results are consistent with the simulation results in that they also indicate that, for bulk wafers with high substrate resistivity, fully silicided multi-finger structures will show uniform triggering due to substrate coupling effects, even with $V_{t2} < V_{t1}$.

Conclusion

In this paper, we have presented a multi-finger turn-on model incorporating substrate coupling effects in a multi-finger structure. We have demonstrated the importance of the starting material for triggering uniformity and thus current handling capability of multi-finger transistors. The experimental and simulation results provide insight into the nature of uniform triggering, and show the possibility of using fully silicided transistors as an ESD protection device without any process/design modifications.

References

[1] Thomas L. Polgreen, et al., IEEE TED-39, pp. 379, 1992.

[2] Markus P. J. Mergens, et al., ESD/EOS Symposium 2001, pp. 1.

[3] Ajith Amerasekera, et al., IEEE TED-38, pp. 2161, 1991.

[4] SEQUOIA Device Designer User's Guide, SEQUOIA Design Systems, 1998-2001.

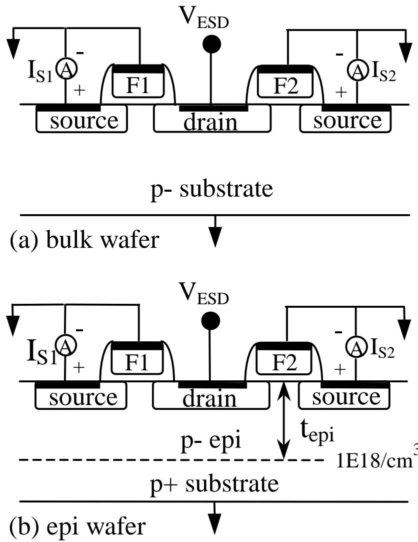


Fig. 1 – Cross section of multi-finger NMOS transistors. Note that F1 has a 10% lower channel doping than that of F2.

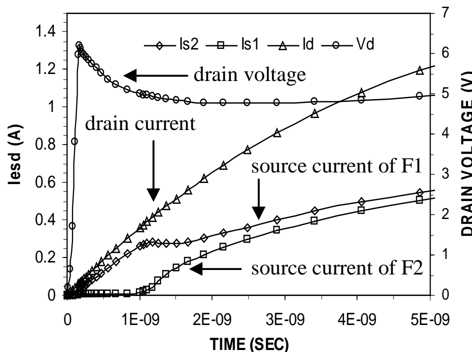


Fig. 2 – The current waveforms along with the drain voltage for bulk wafer case.

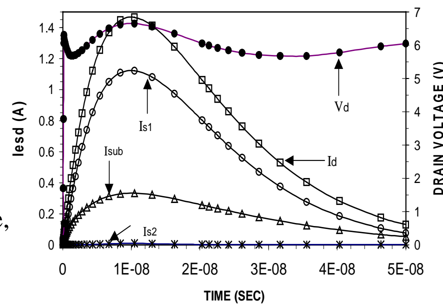


Fig. 4 – The current waveforms along with the drain voltage for epi wafer. Note that F2 (I_{s2}) doesn't trigger.

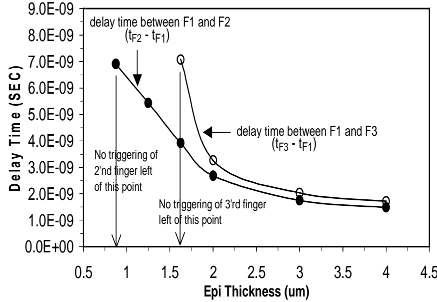


Fig. 6 – Triggering delay as a function t_{epi}. Three fingers of NMOS were used in this simulation.

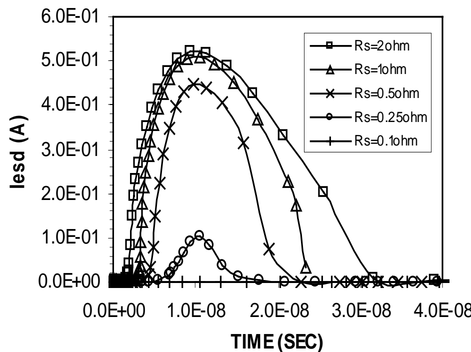


Fig. 8 – Simulation results for multi-finger triggering as a function of source resistance (Rs) shown in Fig. 7. The source current (I_{s2}) of the second finger was measured.

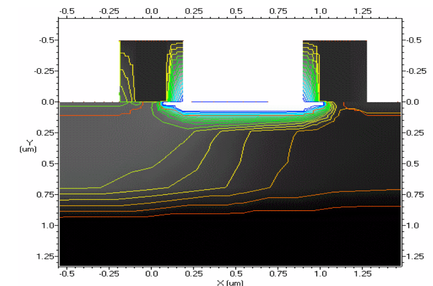


Fig. 5 – Potential contours at the peak of ESD current (t=10ns) for two finger structure. The t_{epi} is 0.75µm. No substrate coupling occurs.

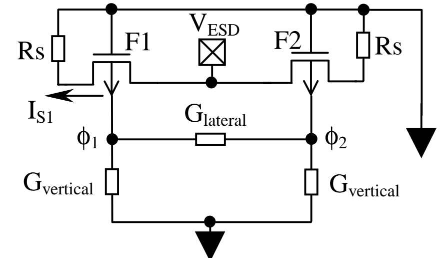


Fig. 7 – Representation of multi-finger turn-on model. The multi-finger triggering occurs when lateral conductance is greater than vertical conductance ($G_{lateral} > G_{vertical}$).

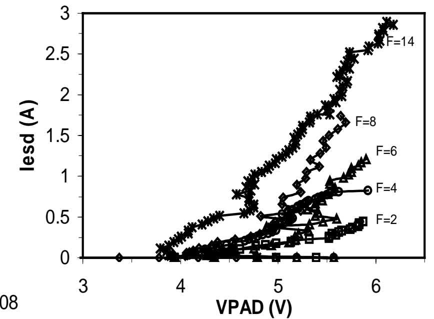
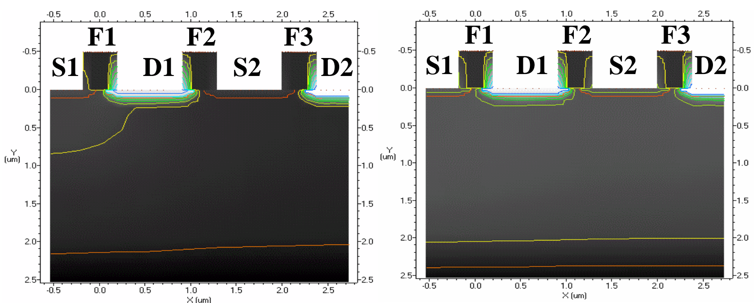


Fig. 9 – TLP I-V characteristics for multi-finger structures having 2, 4, 6, 8,and 14 poly fingers which are 25µm wide with channel length of 0.18µm. I_{t2} level of 8mA/µm was obtained.



(a) right after F1 trigger (at t=1ns) (b) at the peak of ESD current (at t=10ns)

Fig. 3 – Potential contours of multi-finger structure on bulk wafer. Potential contours spread out from the first finger (F1) and reach the second finger to trigger it. The third finger turns on with the same mechanism (domino-effects).

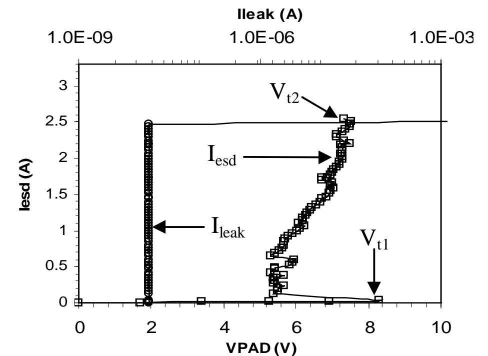


Fig. 10 - TLP I-V characteristics measured from real IO with silicided NMOS as a self protecting output driver. The width is 360um and length is 0.24µm. Note that V_{t1} is larger than V_{t2}.