

# SEQUOIA ESD

## Cascoded NMOS Output Buffer Design

AppNote 2001ESD02

### OVERVIEW

Increasing parasitic bipolar trigger voltage is an effective way to protect a fragile output buffer from ESD damage by making sure the main ESD protection device triggers first. A cascode configuration of two MOSFETs in series as shown in Fig. 1 provides one solution to this problem [1].

SEQUOIA Design Systems' ESD software was used to analyze the performance of the fully isolated cascoded structure.

### MOSFETS

0.18 $\mu$ m devices for this study were created using SEQUOIA Device Designer

software (Fig. 2). Complete parametrization of device geometry, doping and

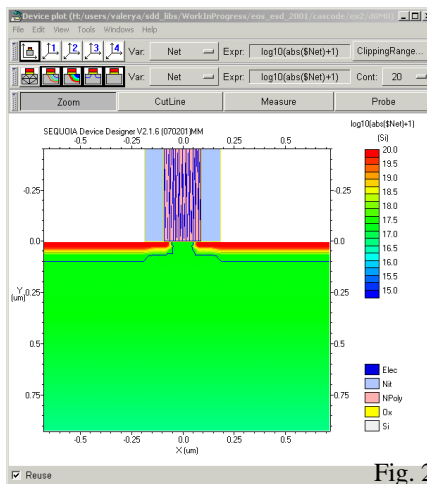


Fig. 2

finite-element triangulation assures ease-of-use. Excellent agreement

between simulation and Transmission Line Pulse (TLP) measured data was achieved without any adjustments to physical coefficients (Figs. 3, 6).

High current behavior is particularly important for an ESD protection device since much of device operation during an ESD event is in this regime. Simulation results match experimental data for all regions of the current-voltage curve.

The MOSFET enters breakdown at about 7V.

The goal of the cascode configuration is to increase the trigger voltage of the parasitic bipolar to make sure it is higher

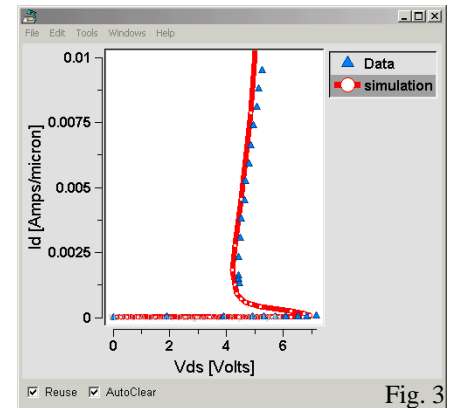


Fig. 3

than the trigger voltage of a typical grounded-gate MOSFET ESD protection device.

### TEST CIRCUIT

A mixed-mode test circuit (Fig. 1) was set up for the analysis of the cascoded structure. Voltage waveforms and currents were extracted during the transient simulation. One possible degree of design freedom for the cascode is the gate bias  $V_g$  applied to the upper MOSFET. Resistors R3, R4 were used to set the gate bias to either a fixed value or tie it to IO pad potential.

### RESULTS

The cascode was subjected to a 2000V Human Body Model (HBM) pulse. The gate of the upper MOSFET was first tied to IO pad potential. Voltage waveforms

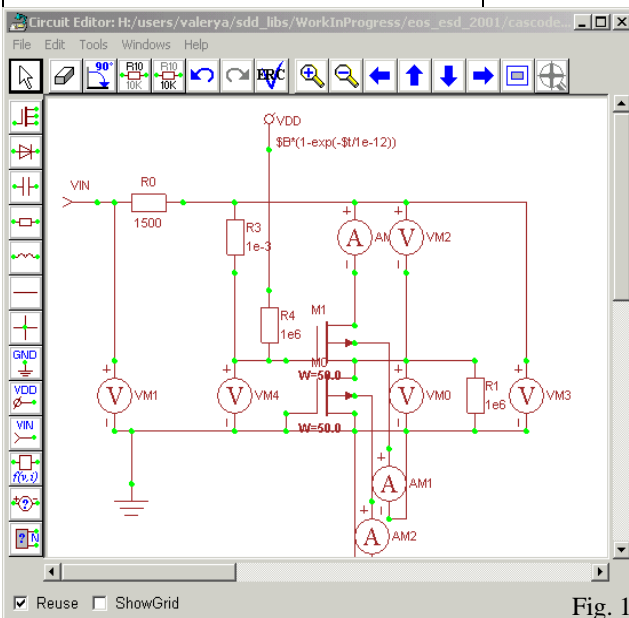


Fig. 1

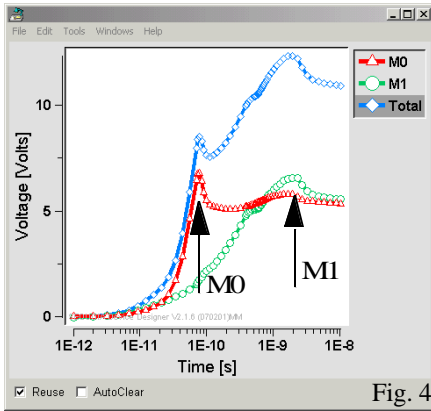


Fig. 4

on the two MOSFETs, as well as the output voltage, demonstrate that the overall trigger voltage is in fact increased significantly from 7V to about 13V. The VSS device M0 triggers first, followed by device M1 with some delay during which the voltage across device M1 is building up to its breakdown value of 7V. Since at this time device M0 is already in snapback-mode, the voltage drop across M0 is smaller than its breakdown voltage of 7V (Fig. 4).

Further increase of the the trigger voltage of the fully isolated cascode is possible by reducing the gate bias  $V_g$  of the upper MOSFET. This is due to an increase in breakdown voltage of the upper MOSFET at lower gate biases. Current-voltage curves extracted from the transient simulation of the cascode for different gate biases  $V_g$  are shown in Fig. 5. In all cases the overall trigger voltage is substantially higher than the

trigger voltage of a single MOSFET (7V).

The behavior of the cascode is significantly different for  $V_g < 7.5V$  from that for higher gate biases. Overall trigger voltages as high as 17V are achieved at low  $V_g$ , when the upper MOSFET is turned off up to its breakdown. For high  $V_g$  values, the upper transistor M1 conducts significant current starting at breakdown of the lower MOSFET M0 and the overall breakdown voltages are lower at about 13V.

The lowered trigger voltage at higher gate biases is due to a reduction in breakdown voltage of the upper MOSFET, as shown by a set of breakdown curves for a range of gate biases (Fig. 6).

These results are valid for the fully isolated cascode structure. A different optimum choice for the gate bias was reported for the case of minimum spac-

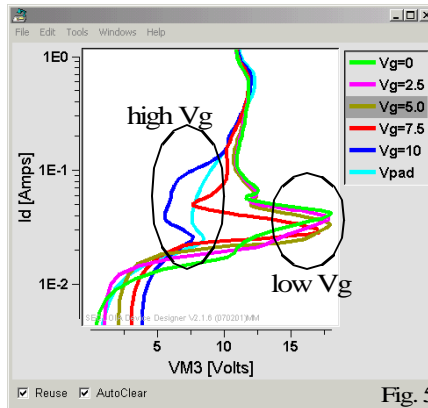


Fig. 5

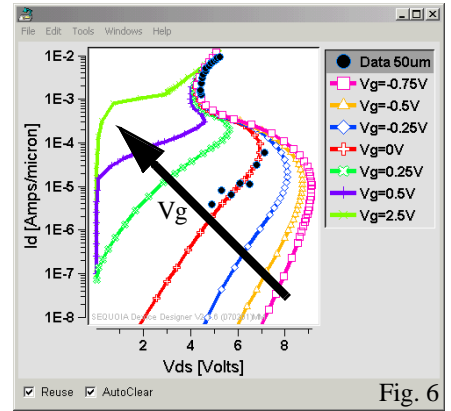


Fig. 6

ing between M0 and M1 due to coupling between the devices [1].

## SUMMARY

Cascoding MOSFETs can be an effective way to increase the trigger voltage of the parasitic bipolar device and help protect fragile NMOS output buffer devices. SEQUOIA ESD offers a complete integrated software solution for the analysis and design of ESD protection circuits. Physical accuracy and ease-of-use are provided in a uniquely powerful package. For more information please contact SEQUOIA Design Systems.

## REFERENCES

- [1] J.W. Miller, M.G. Khazhinsky, J.C. Weldon, Engineering the Cascoded NMOS Output Buffer for Maximum  $V_{t1}$ , EOS/ESD 2000, pp. 308-317.

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