SEQUOIA ESD

Physical Simulation of Charged Device Model ESD Events

AppNote 2001ESD04

OVERVIEW

Deep-submicron semiconductor products exhibit increasing sensitivity to Charge Device Model (CDM) ESD tests. Dielectric failure of fragile core logic MOSFETs can be the result of high currents and voltage build-up occuring internally during a CDM test.

Simulation of CDM events is complicated by the crucial importance of the specific chip layout. Internal voltage build-up depends on current paths taken by the charge accumulated inside the chip and escaping to the grounded IO pad. Chip-level simulation of the CDM event is possible using the approach suggested in [1], where a number of interconnected on-chip circuit blocks are represented by equivalent capacitive circuits. The approach has been applied here using the SEQUOIA ESD software package.

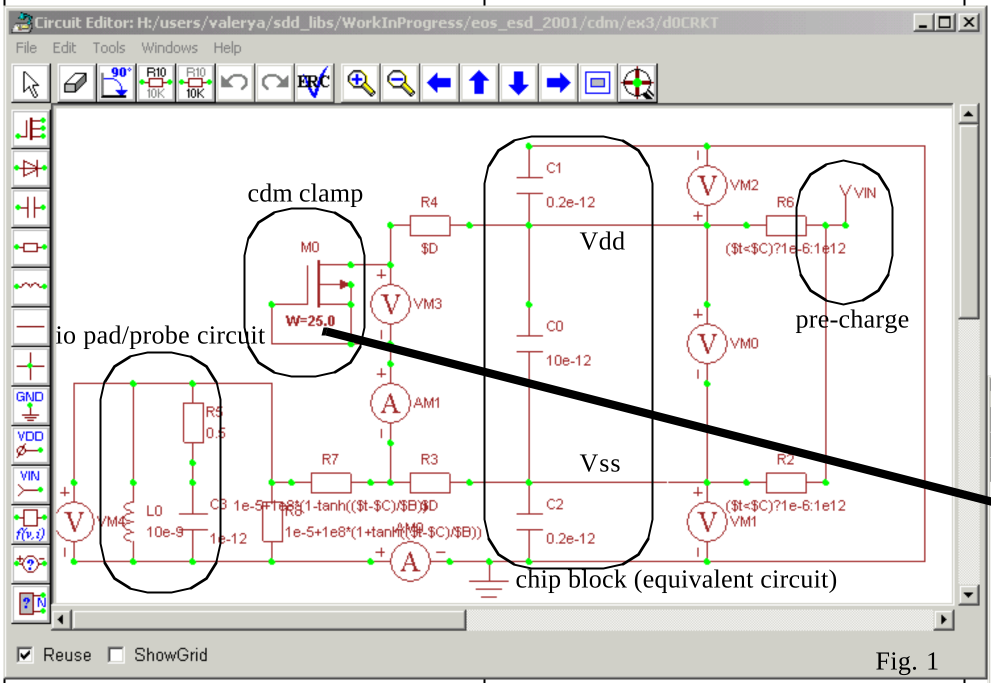

Fig. 1

CHIP-LEVEL CDM

The curcuit used for chip-level simulation of a CDM event contains a three-capacitor network representing an on-chip circuit block (Fig. 1): Cds capacitor C0 (10pF), Cdd capacitor C1 (0.2pF) and Css capacitor C2 (0.2pF). Internal charge storage on the circuit block is modeled by these capacitors. Pre-charging to CDM test voltage of 500V is accomplished via the VIN node, connected to the capacitor network by time-dependent resistors R2, R6.

A CDM event is simulated by discharging the capacitor network into the equivalent pad circuit L0 (10nH), R5 (0.5 Ohm), C3 (1pF). Charge sharing between Cds and Cdd produces a voltage difference Vds during the discharge. Additional internal voltage build-up occurs due to voltage drop on power rails represented by R3, R4. An internal CDM clamp M0 (W=25?m, Fig. 2) is placed between the power rails to limit the voltage difference to safe levels.

A transient mixed-mode simulation is carried out using SEQUOIA ESD software to calculate the internal current and voltage waveforms and to determine the resulting voltage build-up during the CDM discharge. Protective action of the ESD clamp M0 is assessed by a comparison of internal voltage

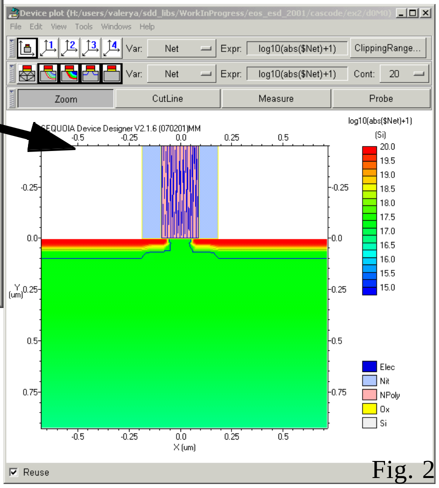

Fig. 2

waveforms with and without the clamp device.

CALIBRATING THE MOSFET

The CDM protection clamp is simulated as a physical finite-element model embedded in a mixed-mode circuit. A parametrized device structure, doping profiles and fully automatic mesh generation were used (Figs. 2, 3).

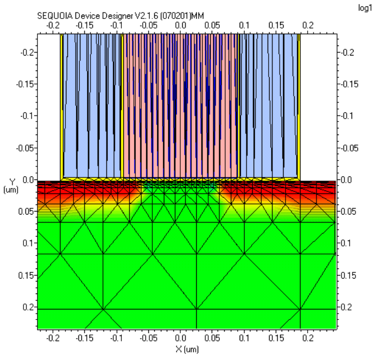

Fig. 3

For the simulation to be realistic, it is important to verify the accuracy of the MOSFET simulation particular with respect to breakdown. A comparison of simulation to experimental Transmission Line Pulse (TLP) data (Figs. 4,5) provides this verification.

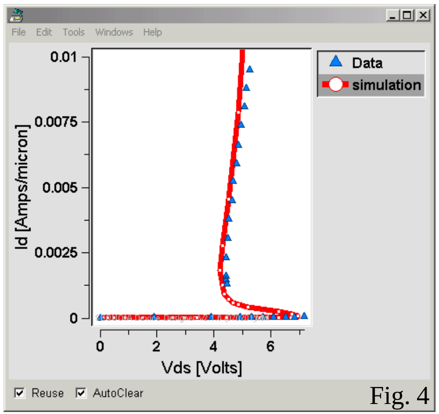

Fig. 4

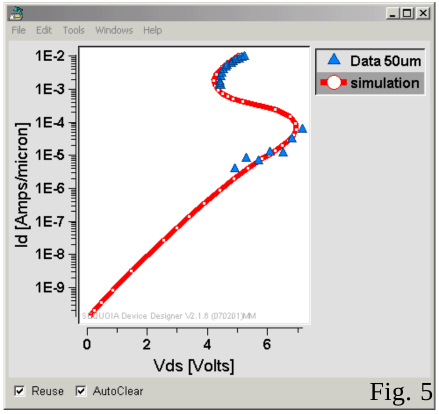

Fig. 5

TRANSIENT SIMULATION

Transient mixed-mode simulations were carried out with and without the grounded-gate MOSFET M0. After pre-charging the circuit to 500V, a discharge path was created via the time-dependent resistor R7 acting as a switch. Due to the low parasitic resistance R5 of the probe and its inductance L0, the discharge current shows rapidly oscillating behavior (Fig. 6).

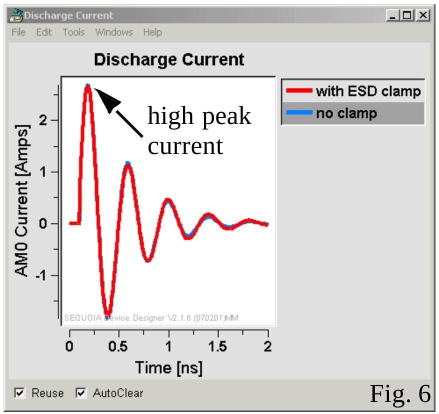

Fig. 6

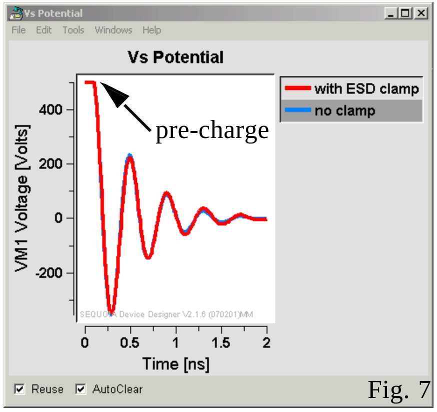

Fig. 7

Internal chip potentials Vss and Vdd follow the same pattern of damped oscillation starting at the pre-charge voltage Vcdm=500V (Fig. 7). Charge sharing between Cds and Cdd results in a voltage difference Vds [1]:

$$V_{DS} = \frac{C_{DD}}{C_{DS} + C_{DD}} V_{CDM} \quad \text{(EQ 1)}$$

In our case we observe a peak Vds of about 17V, a dangerously high value for thin dielectrics in submicron MOSFETs.

If the discharging circuit block (represented by the capacitor network Cds, Cdd, Css) is located a significant distance away from the current sink (IO pad), additional voltage build-up can occur due to voltage drop on power rails. A 4Ohm line resistance R3,R4 leads to an unclamped peak voltage of 22V (Fig. 9). This voltage spike would lead to permanent oxide failure of fragile core logic devices.

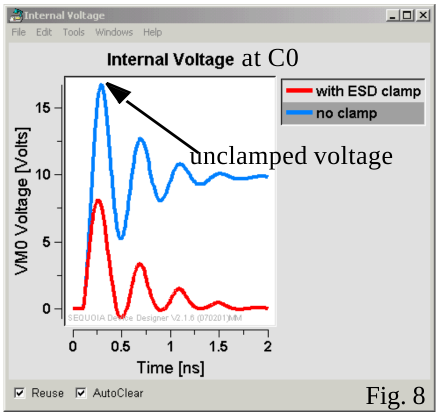

Fig. 8

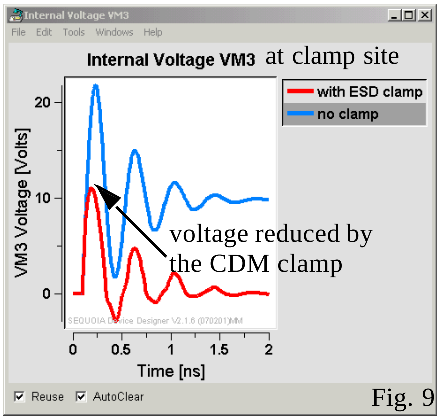

Fig. 9

A grounded-gate MOSFET was placed in the circuit as a small CDM clamp M0 with a device width of W=25?m to limit the peak internal voltage build-up to safe values. Mixed-mode simulation results demonstrate that the CDM clamp triggers (Fig. 10) to limit the internal voltage

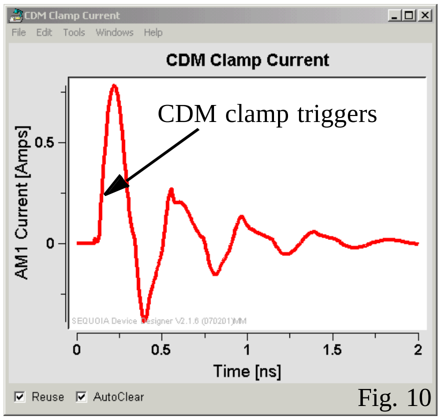

Fig. 10

build-up to about 10V at the CDM clamp site (Fig. 9). Circuit designers can use such findings to determine where CDM clamps need to be placed to assure safe handling of CDM events.

Realistic CDM applications can include multiple circuit blocks represented by capacitive networks Cds, Cdd, Css with complex discharge current flows between them as demonstrated in [1]. The circuit in Fig. 11 is an example of a two-block multi-power IC CDM problem, where charge collected in block A passes through block B on its way to the grounded pin.

SUMMARY

Charged Device Model ESD events are a substantial challenge for modern deep-submicron integrated circuits. Analysis of the CDM event is complicated by the layout-dependent current flow and voltage build-up inside a chip.

Chip-level simulation of CDM events is necessary to capture the relevant effects. Mixed-mode physical simulation provides an accurate description of the discharge event and the protective capabilities of distributed ESD clamps.

SEQUOIA ESD offers a complete integrated software solution for the analysis and design of ESD protection circuits. Physical accuracy and ease-of-use are combined in a uniquely powerful package. For more information please contact SEQUOIA Design Systems.

REFERENCES

[1] J. Lee, Y. Huh, J.-W. Chen, P. Bendix, S.-M. Kang, Chip-Level Simulation for CDM Failures in Multi-Power ICs, EOS/ESD 2000, pp. 456-463.

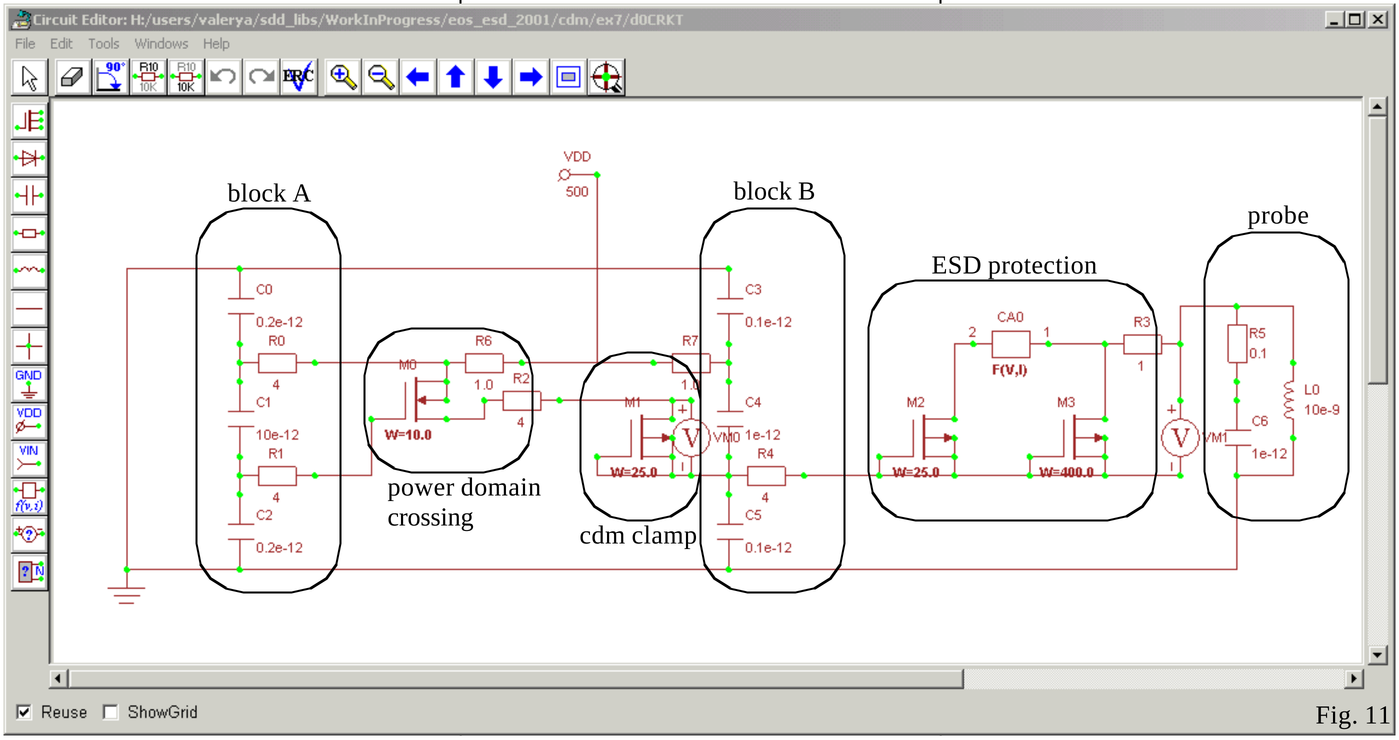

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Fig. 11

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