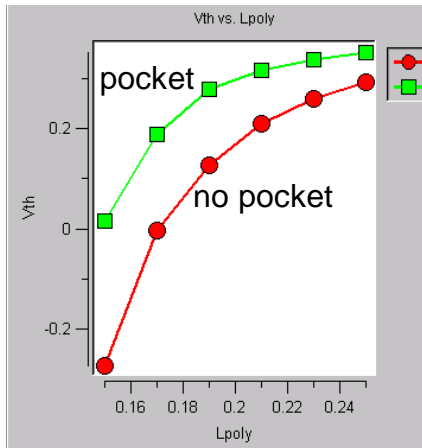


Design for Manufacturability: Controlling Performance and Variability

SEQUOIA Design Systems, Inc.

Semiconductor manufacturing is subject to intrinsic variations, which cause active device variability and de-grade circuit performance. Since a certain level of manufacturing variations is unavoidable, a manufacturable device design is one that is sufficiently insensitive to these variations.

The major source of device variability is polysilicon gate length variation, which can be as high as

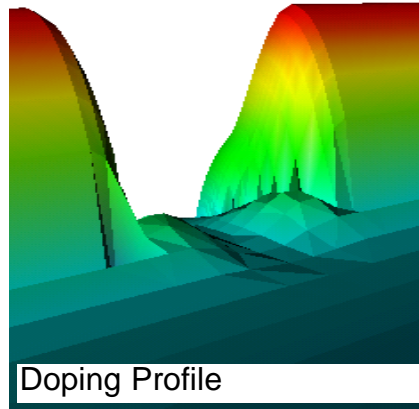


10% of nominal value. Controlling the device sensitivity with respect to L_{poly} variability is therefore crucial to achieve a stable and manufacturable device design.

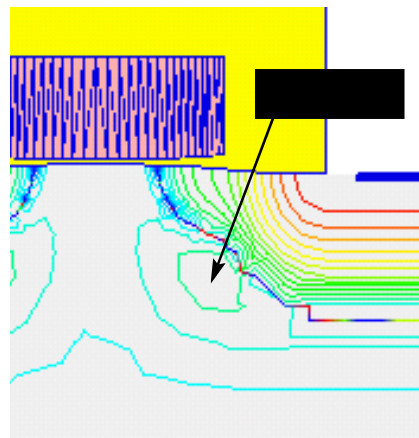
A so-called pocket or halo implant is a common technique to reduce the sensitivity of device performance to gate length. A recent application of this technique is described in [1]. This implant surrounds the source/drain junctions and thus reduces punch-through leakage. The pocket implant must be carefully optimized to fully realize its potential. The effectiveness of the pocket implant strongly depends on its peak concentration,

depth and the amount of gate underlap controlled by the implant tilt angle.

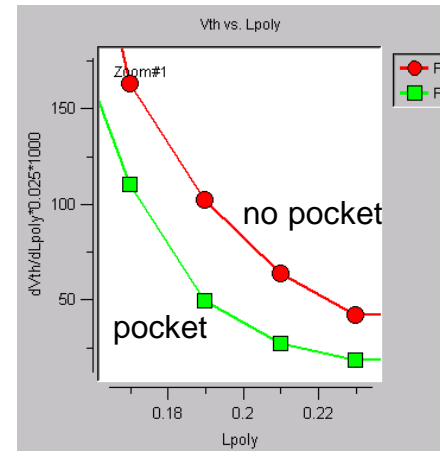
A well-designed pocket implant



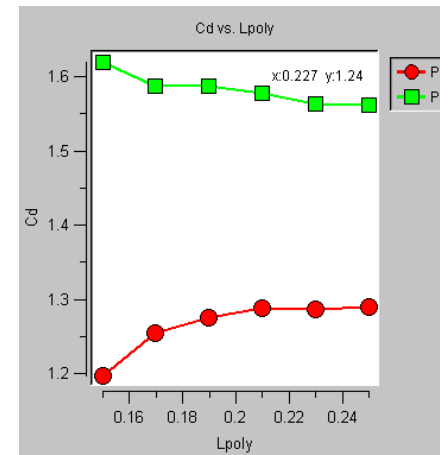
can substantially reduce the short-channel effect at the target gate length and reduce the sensitivity of



the device to unavoidable variability of the gate length. This sensitivity is measured by the slope of the V_{th} vs. L_{poly} curve. In the example in the right corner, the expected V_{th} variability is displayed in mV given an L_{poly} variability of 0.025 μm. At a target L_{poly} of 0.2 μm, the pocket implant lowers the expected V_{th} variability from 75 mV to 35 mV.



On the other hand, the pocket implant increases the device's junction capacitance as shown in the figure below and can result in an overall degradation of speed performance.



SEQUOIA Device Designer allows to determine which device architecture assures optimal performance combined with low sensitivity to manufacturing variations. Its speed and ease-of-use allow the entire optimization process to be carried out quickly and with exhaustive coverage of all possibilities.

[1] A. Brand et al., "Intel's 0.25 Micron, 2.0Volts Logic Process Technology," Intel Technology Journal, 3rd Quarter 1998