

# Inverse Modeling Intel's 130nm NMOS and 150nm PMOS

## Internal Memo

SEQUOIA Design Systems

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### Summary

Current status of ongoing efforts on inverse modeling Intel's IEDM98 130nm NMOS and 150nm PMOS high-performance logic technology:

- A TCAD model of the device was constructed in SEQUOIA Device Designer including shallow source/drain extensions, a channel implant, halo implant. The model takes poly gate depletion and quantum mechanical effects in the channel inversion layer into account. Meshing is automated and inverse modeling is carried out in a series of optimization steps. Lombardi and Caughey-Thomas mobility models are used.
- Good agreement with measured data was achieved for a number of key measurements including subthreshold curves, DIBL,  $V_{tlin}$ ,  $V_{tsat}$ , drain curves,  $I_{off}$ ,  $I_{dsat}$ . The only physical model coefficient which was adjusted is electron saturation velocity (from  $1.07e7$  to  $1.19e7$  cm/s,  $1.16e7$  cm/s for holes). This may be justified by the presence of a velocity overshoot due to very short channel length of the device (NMOS:  $L_{poly}=130nm$ ,  $L_{eff}=85nm$ ).

TABLE 1. Measured data and simulation results

Parameter	Measurement [1]		Simulation	
	NMOS	PMOS	NMOS	PMOS
$T_{eff}$ (measured in inversion)	30A	30A	30A	30A
Poly gate doping concentration	unknown	unknown	$8e19 \text{ cm}^{-3}$	$8e19 \text{ cm}^{-3}$
$T_{ox}$ (physical)	unknown	unknown	26A	26A
$I_{off}$	3 nA/ $\mu m$	3 nA/ $\mu m$	3 nA/ $\mu m$	3 nA/ $\mu m$
$I_{dsat}$	940 $\mu A/\mu m$	420 $\mu A/\mu m$	940 $\mu A/\mu m$	420 $\mu A/\mu m$
$V_{tlin}$	0.4 V	-0.36 V	0.4 V	-0.36 V
$V_{tsat}$	0.29 V	-0.24 V	0.24 V	-0.2 V
Subthreshold slope	< 90 mV/dec	< 90 mV/dec	81 mV/dec	79 mV/dec
$L_{eff}$	unknown	unknown	85 nm	69nm
Overlap ( $0.5*(L_{poly}-L_{eff})$ )	unknown	unknown	22.5 nm	40.5 nm
$V_{satN}$ (saturation velocity)	unknown	unknown	$1.19e7 \text{ cm/s}$	$1.16e7 \text{ cm/s}$

- Roll-off curves were generated for both NMOS and PMOS. The agreement is better for the PMOS device, less good for the NMOS device. Reasons may include presence of dopant redistribution effects not taken into account by the parametrized TCAD model in SDD.

- A remaining issue is that the extracted gate to drain capacitance is higher than reported in Intel's oral presentation (0.5fF/um instead of 0.27fF/um) despite a small gate-to-drain overlap of 22.5nm for the NMOS device. This capacitance is reduced if gate non-planarity is assumed to be present. However, it is unclear whether significant non-planarity is present in the manufactured device.

## References

- [1] S. Yang et al., "A High Performance 180nm Generation Logic technology", IEDM 1998

## Tox Calculation from Teff

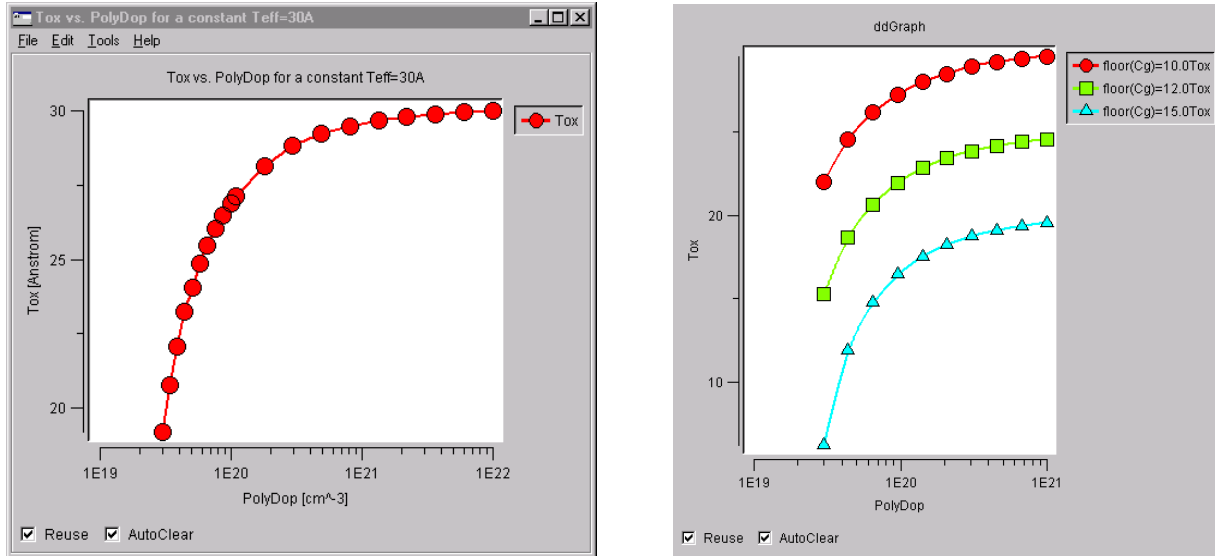


Fig. 1. Oxide thickness for a constant electrically effective  $T_{eff}=30A$  as a function of poly doping.  $T_{eff}$  measured in inversion at  $V_g=1.5V$ . Figure on the right:  $T_{eff}=20,25,30A$  at  $V_g=1.2V$

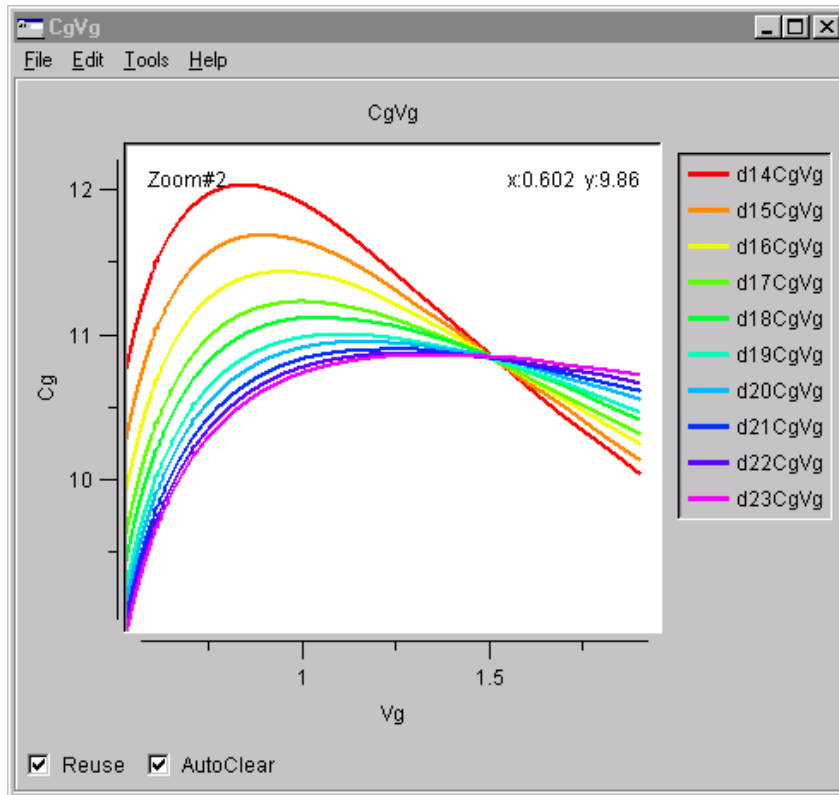


Fig. 2. CV curves for poly doping levels ranging from  $3e19$  to  $1e20$   $cm^{-3}$ .

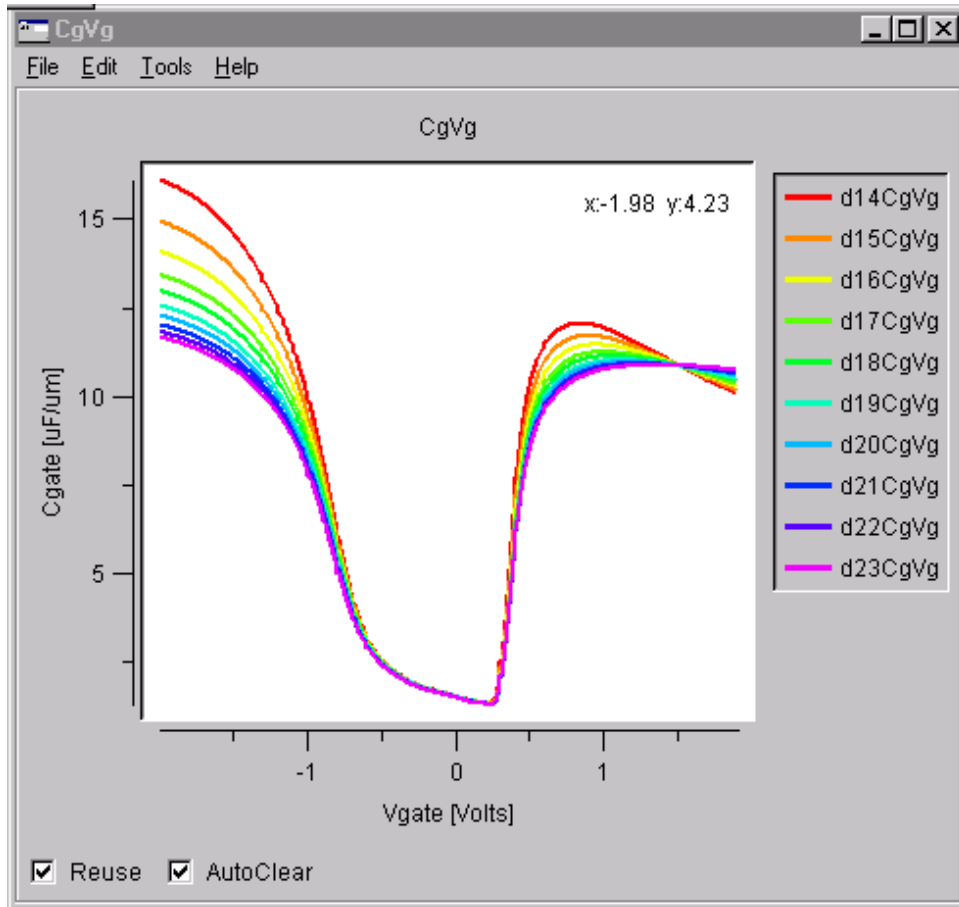


Fig. 3. CV curves for poly doping levels ranging from  $3 \times 10^{19}$  to  $1 \times 10^{20} \text{ cm}^{-3}$ .

## Gate Curves

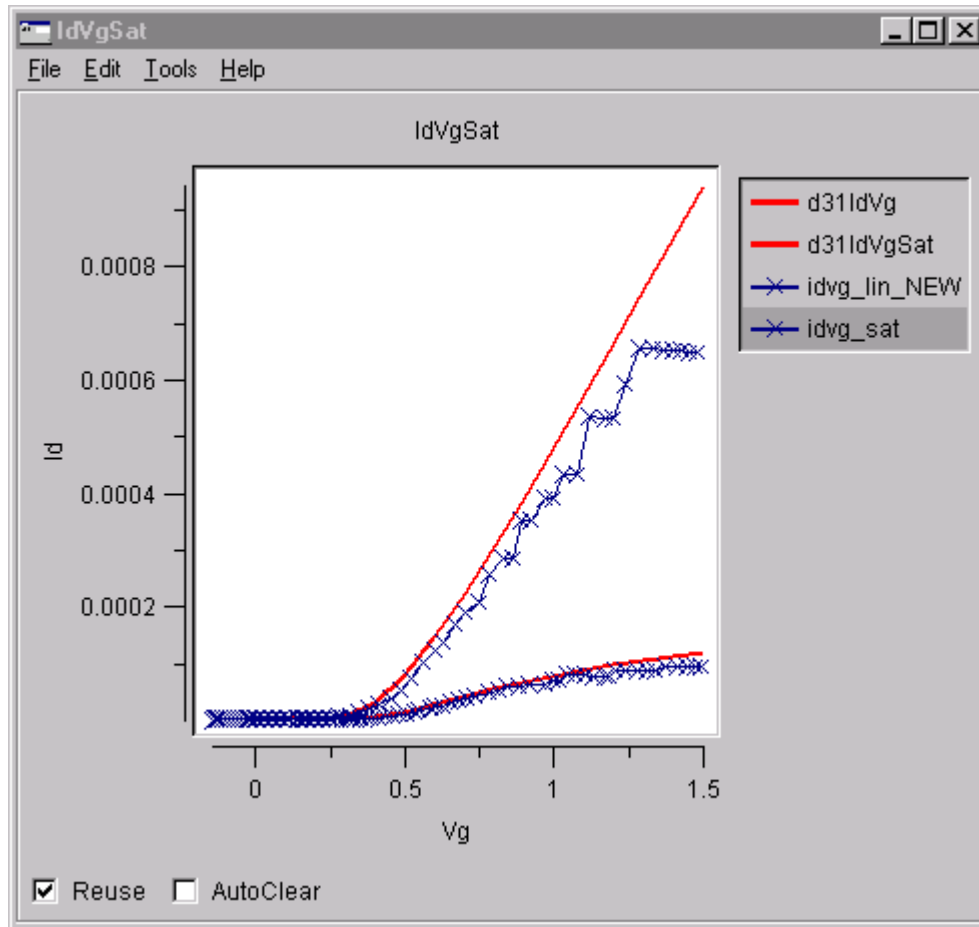


Fig. 4. NMOS gate curves on linear scale. Simulation - lines, data - crosses (data was digitized from a log scale curve in [1], inaccuracies at high current values are evident).

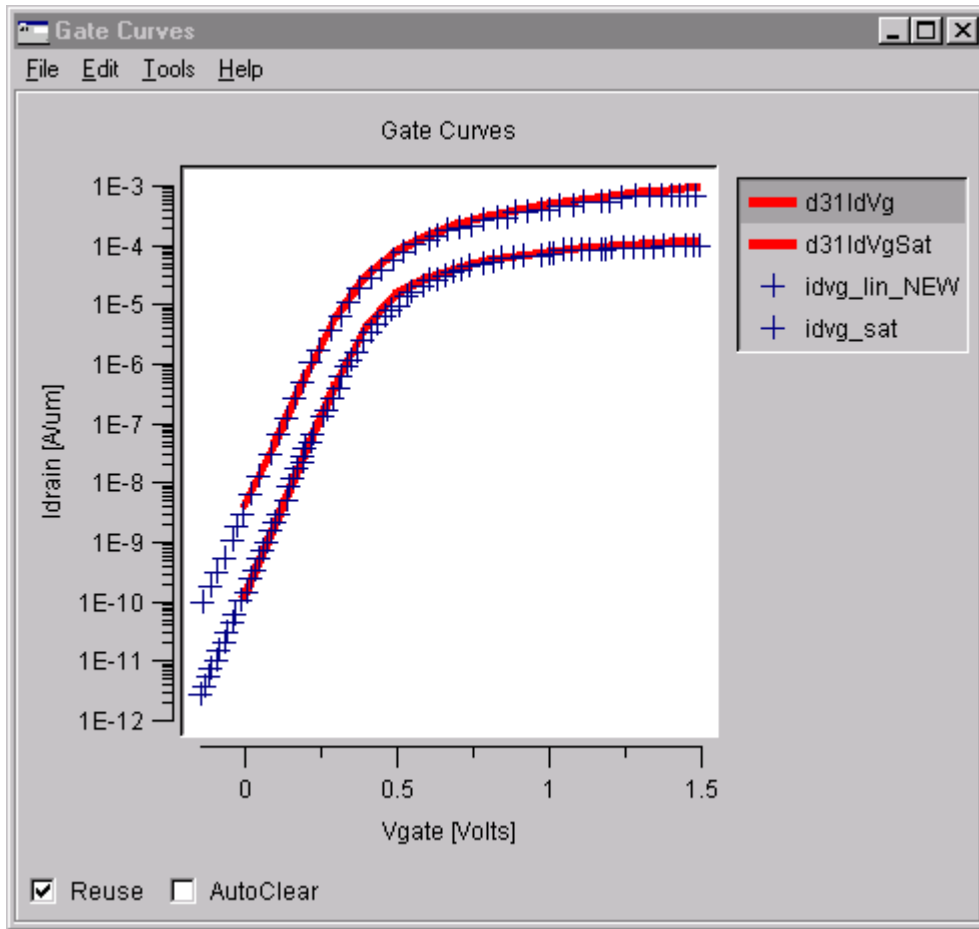


Fig. 5. NMOS gate curves on log scale.

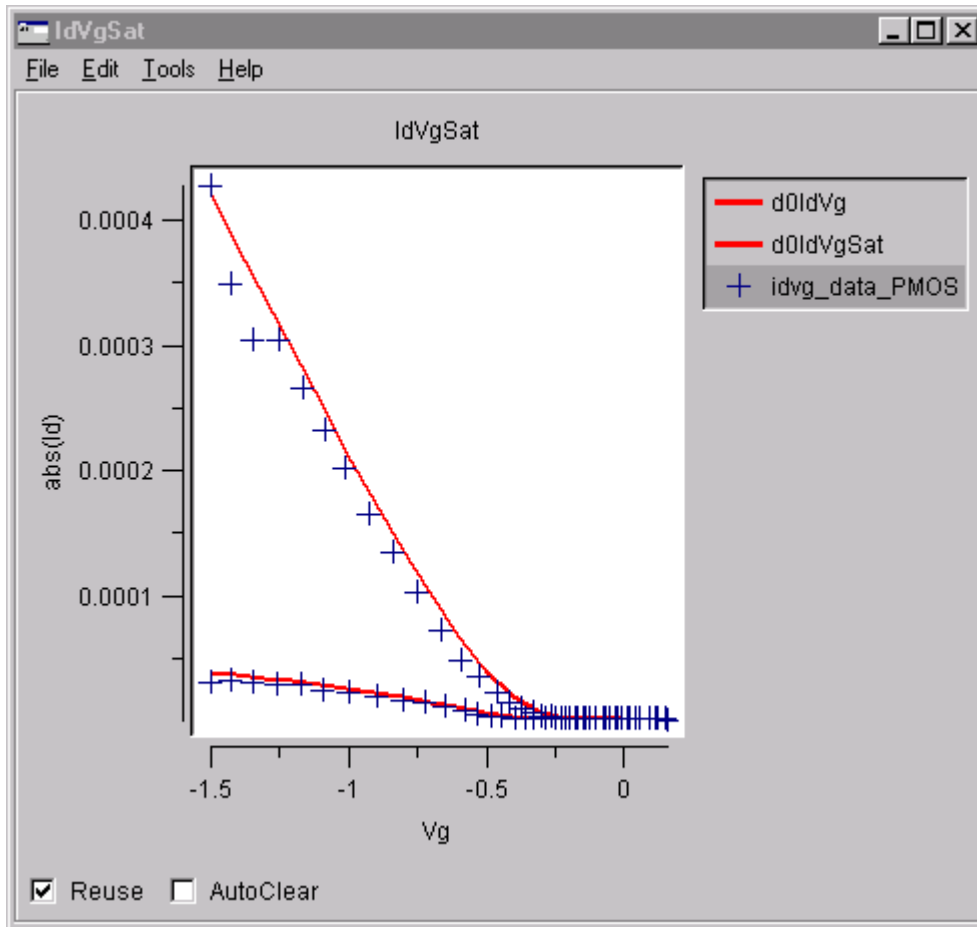


Fig. 6. PMOS gate curves on linear scale. Simulation - lines, data - crosses (data was digitized from a log scale curve in [1], inaccuracies at high current values are evident).

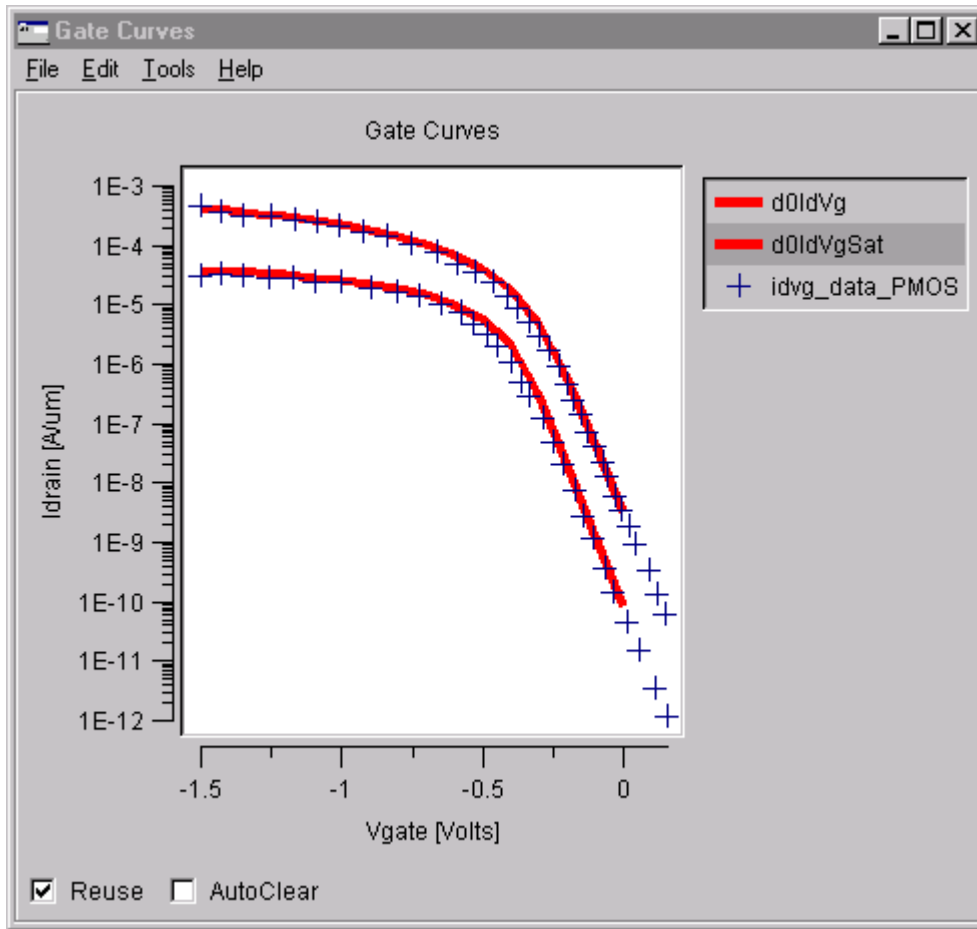


Fig. 7. PMOS gate curves on log scale

## Drain Curves

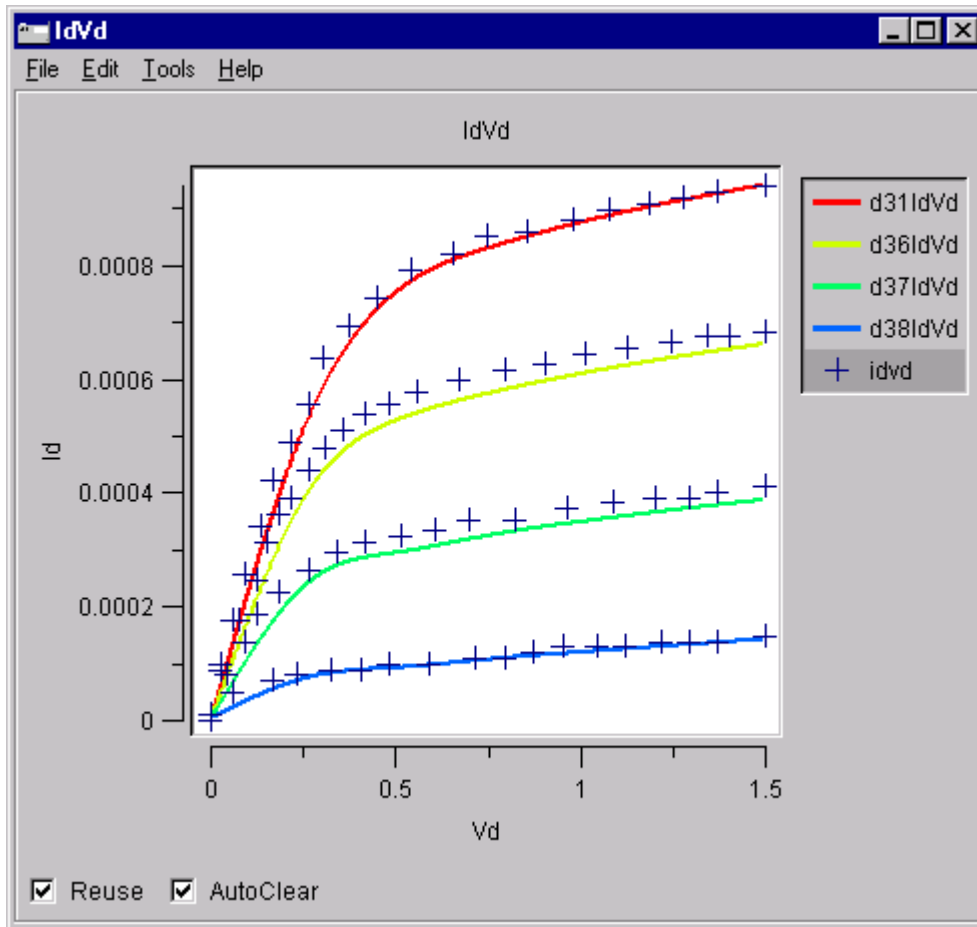


Fig. 8. NMOS drain curves. Simulation - lines, measured data - crosses.

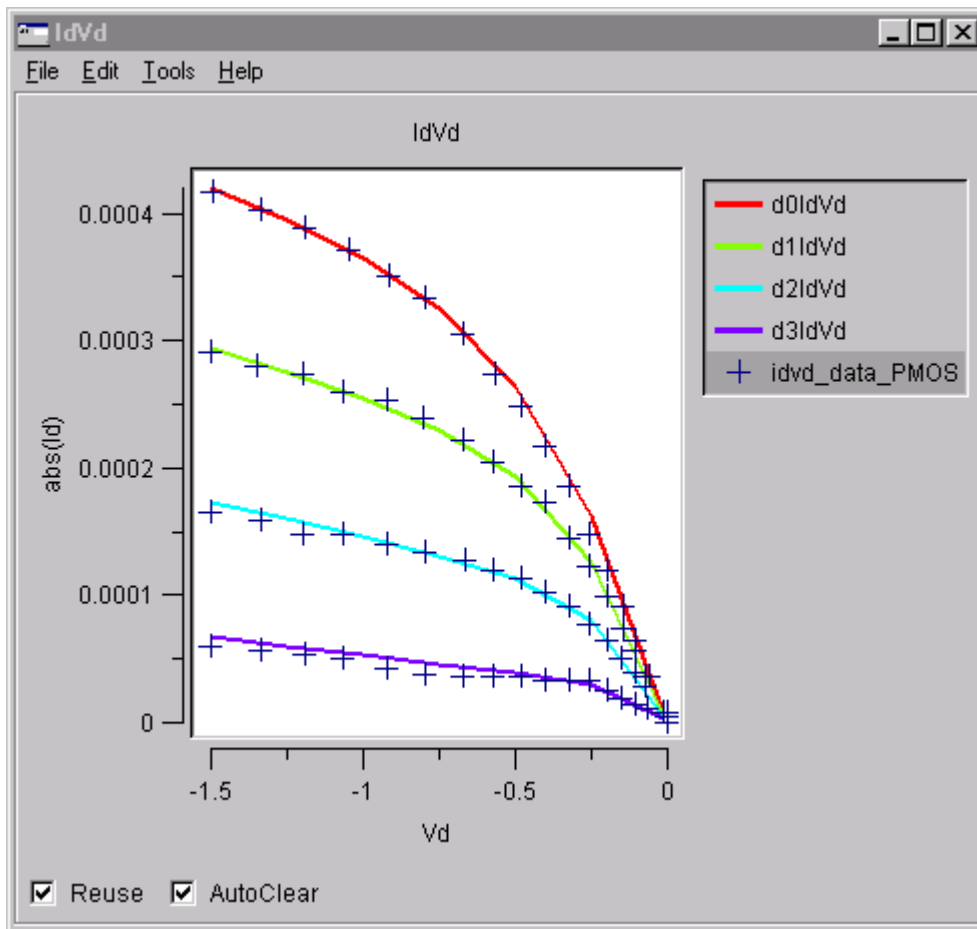


Fig. 9. PMOS drain curves. Simulation - lines, measured data - crosses.

## Roll-Off

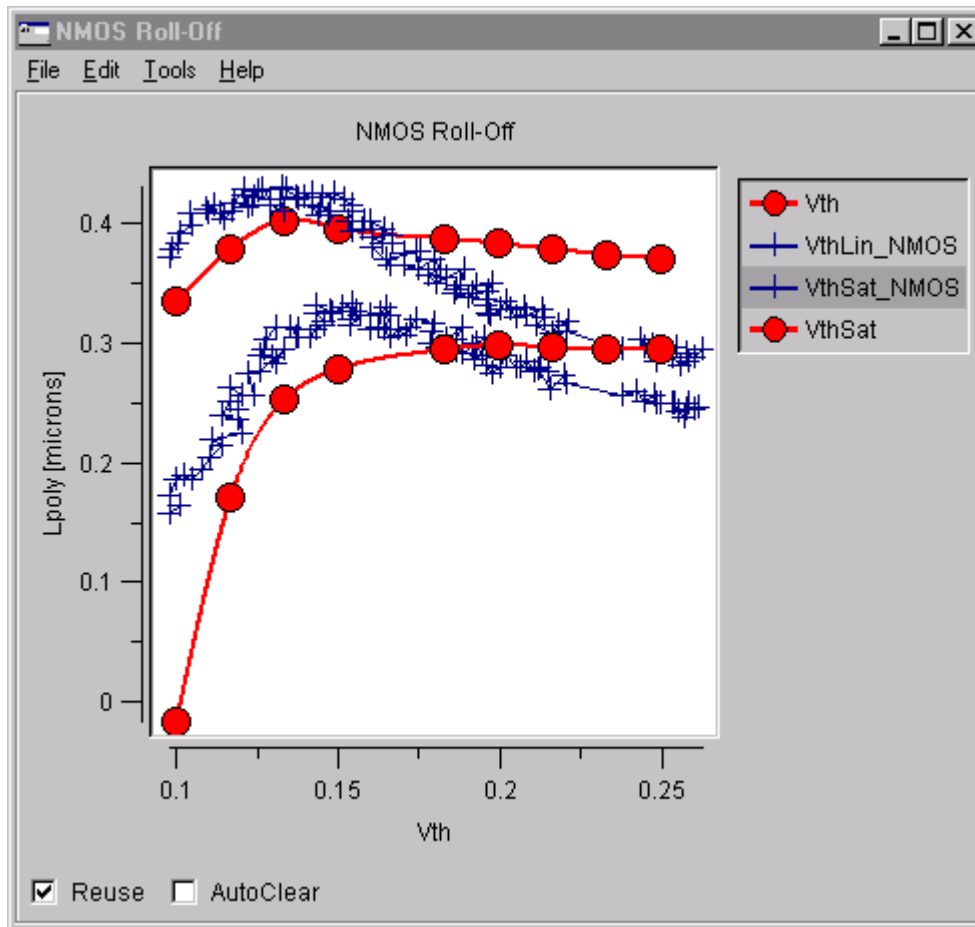


Fig. 10. NMOS Roll-off simulation and experimental data.

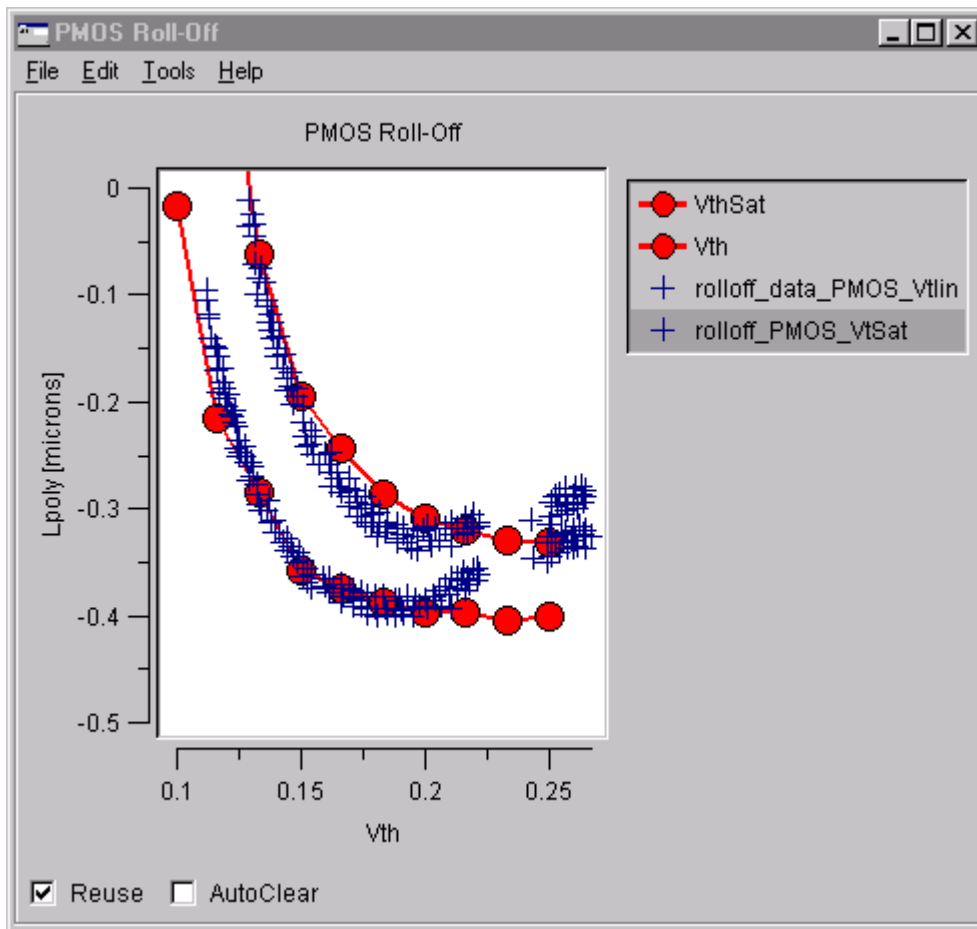


Fig. 11. PMOS Roll-off simulation and experimental data.

## Device Structure

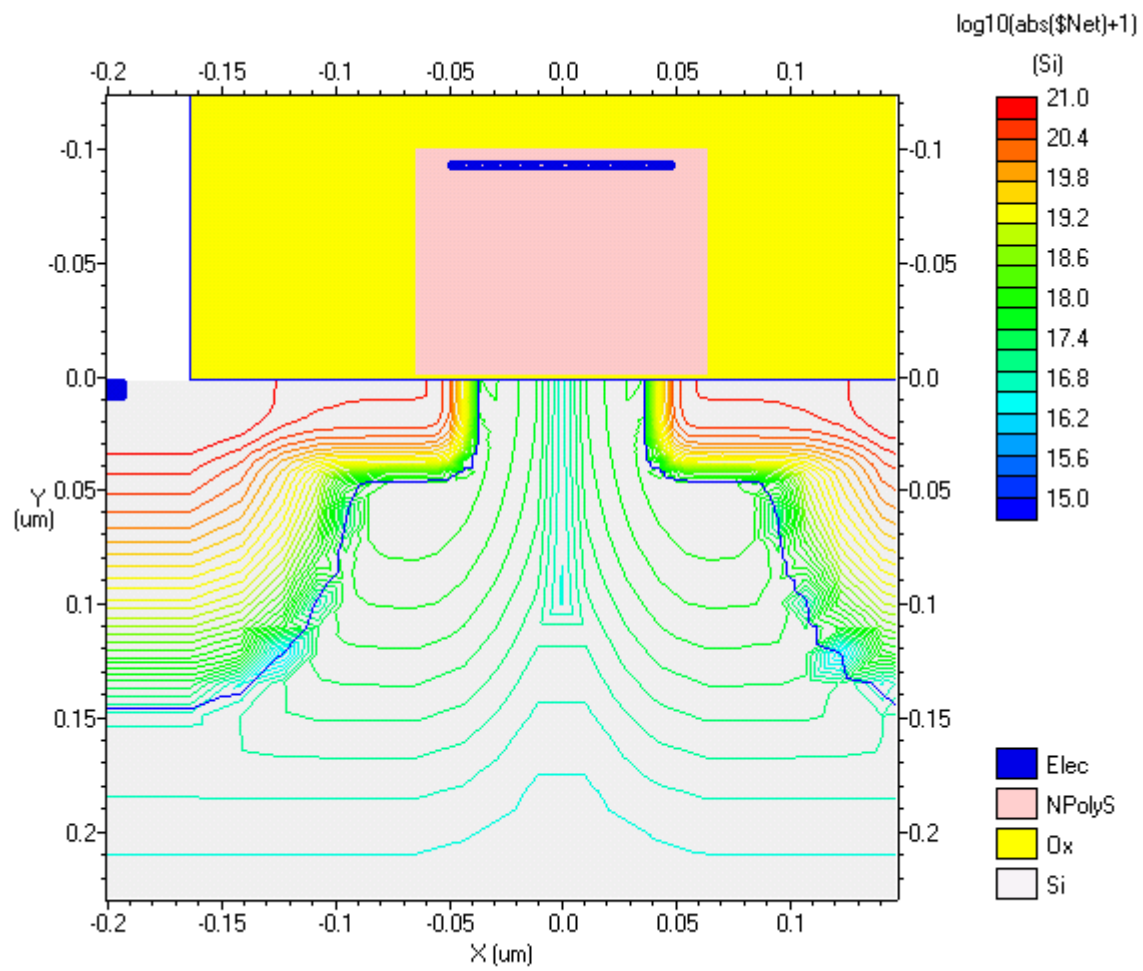


Fig. 12. NMOS device structure and doping contours.

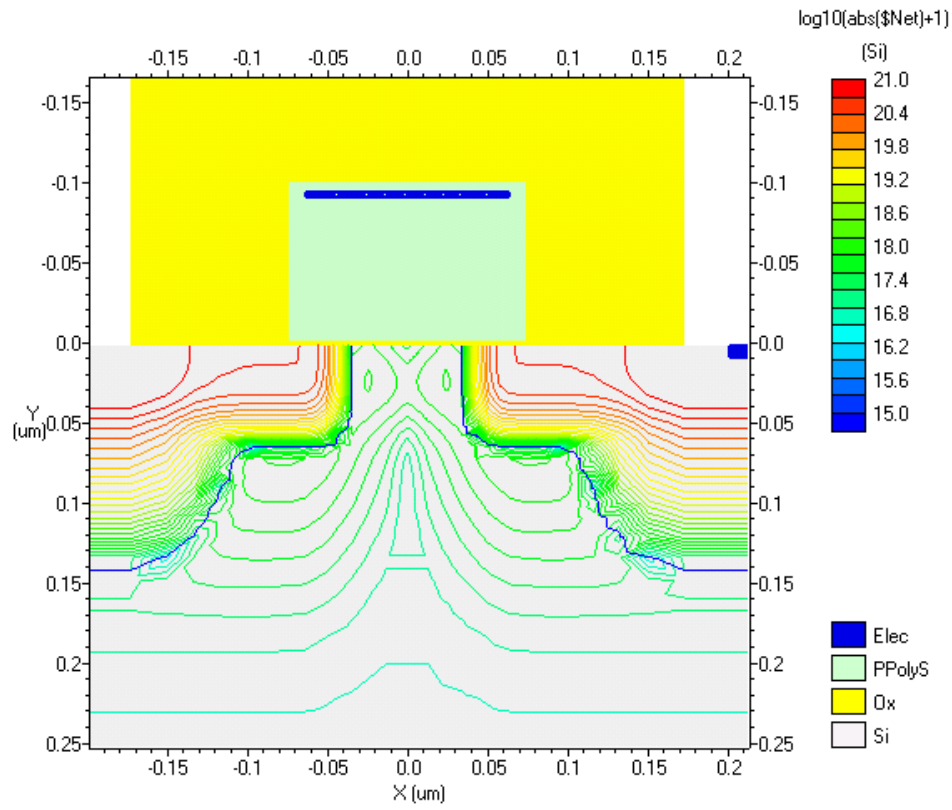


Fig. 13. PMOS device structure and doping contours.