SEQUOIA Device Designer

SCR-Based ESD Protection

AppNote 2003ESD01

OVERVIEW

Silicon Controlled Rectifier (SCR) is a widely used used device for ESD protection. Its advantages include high current handling capabilities and low holding voltage. This application note describes the analysis of an SCR structure used for ESD protection under 2kV HBM stress.

The SCR device is implemented in a

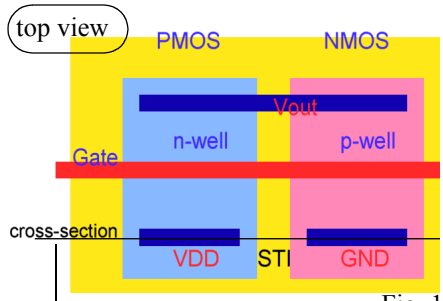

Fig. 1

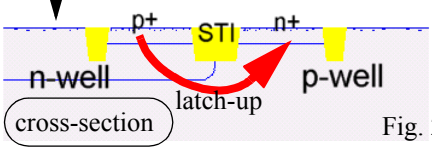

Fig. 2

Shallow Trench Isolation (STI) technology. A top view and a cross-section of a basic CMOS inverter are shown in Figs. 1, 2 respectively. Isolation properties of STI are characterized by calculating the triggering voltage of the parasitic p+npn+ thyristor structure. The latch-up path is indicated by the red arrow in Fig. 2.

SCR SETUP

A parametrized two-dimensional simulation structure, mesh and doping were set up for the simulation as shown in Fig. 3. Also shown is the electric potential in

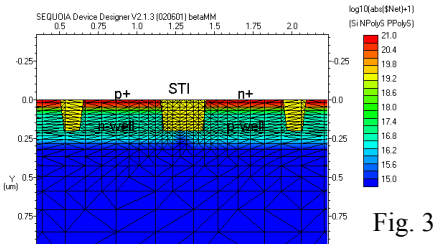

Fig. 3

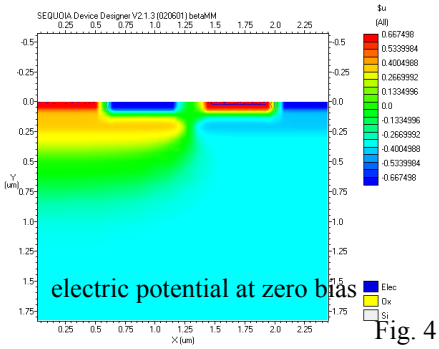

Fig. 4

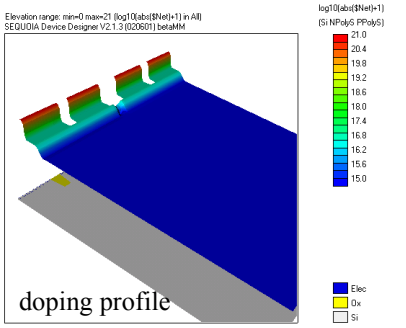

Fig. 5

the structure at zero bias (Fig. 4) and the doping profile (Fig. 5). High built-in potential in n-type regions (n-well and n+) is seen in red colors. Automatic meshing and parametrization of the structure allow in-depth studies of the STI properties with respect to geometry

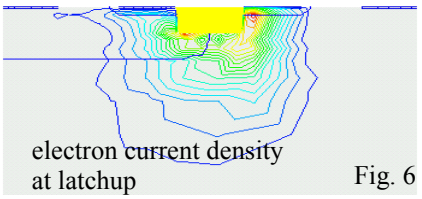

Fig. 6

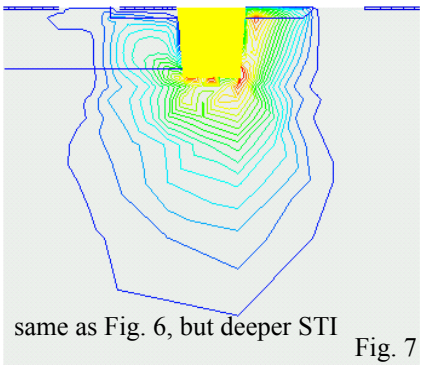

Fig. 7

and doping parameters with little user effort (Figs. 6, 7).

ESD SIMULATION

The SCR device was embedded in a test circuit as shown in Fig. 8. Human Body Model (HBM) stress of 2kV was applied to the input node VIN. The SCR was placed between the VIN node (I/O pad)

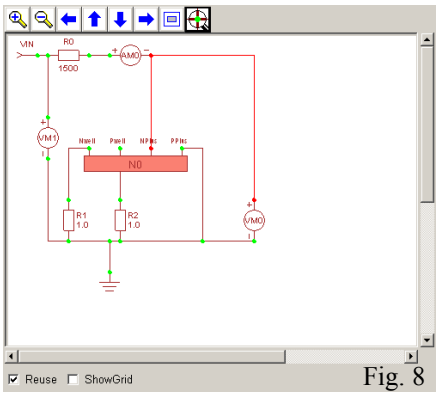

Fig. 8

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and ground. A transient simulation was performed to study the circuit response under HBM stress. The pad voltage during the discharge was captured with the voltmeter VM0. The discharge current was measure using the amperemeter AM0.

RESULTS

The pad voltage VM0 is shown in Fig. 9 on a logarithmic time scale. The SCR triggers at about 0.1ns after the start of the discharge. It then enters snapback with a holding voltage of approximately

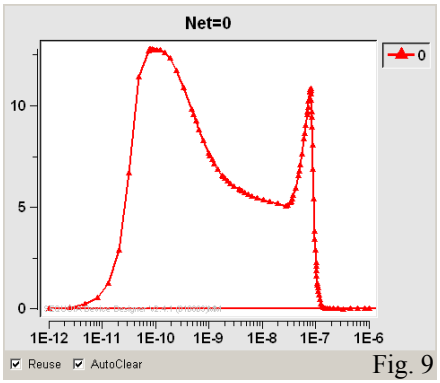

Fig. 9

5V. Further tuning of the SCR and the protection circuit may be needed to reduce the maximum pad voltage to keep it safely below oxide failure levels.

As an example, a full-factorial experiment varied STI depth and width with three settings each: 0.3, 0.45, 0.6?m. Triggering voltages were extracted for each of the 9 settings (Fig. 10).

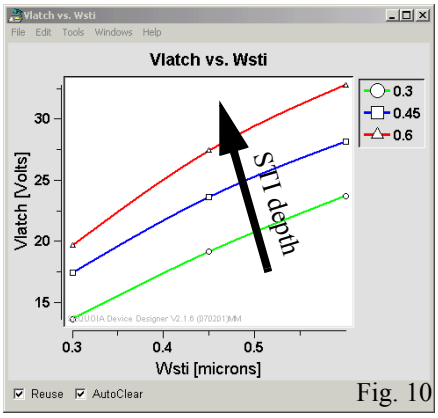

Fig. 10

Trigger voltages were extraced from each transient simulation and summarized in Fig. 10. As expected, results show that both increases in depth and in width improve latch-up susceptibility of STI.

On the other hand, the triggering voltage of the SCR needs to be low enough to protect sensitive thin oxides. To achieve low triggering voltage, a shallow and/or narrow STI is desirable. Sensitivity to other parameters, such as well depth and doping level, STI sidewall slope, etc., can be easily included in the analysis to arrive at an optimal STI.

Embedding the protection device in a larger circuit including parasitic chip capacitances, metal and via resistances and other semiconductor devices can reveal important effects, which can help determine optimal protection device configuration and placement.

SUMMARY

Silicon Controlled Rectifiers are frequently used as ESD protection devices. SCR protection capabilities depend on their triggering voltage, holding voltage and current handling capabilities. Optimal design of SCR protection structures is important for high yields and efficient silicon area utilization. SEQUOIA Device Designer - ESD offers a complete integrated software solution for the analysis and design of SCR-based ESD protection circuits and SCR device structures. Physical accuracy and ease-of-use are combined in a uniquely powerful package. For more information please contact SEQUOIA Design Systems.

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