

# SEQUOIA Device Designer

## Shallow Trench Isolation Analysis and Design

AppNote 2001ESD03

### OVERVIEW

Shallow Trench Isolation (STI) is a standard isolation approach for sub-0.25 micron technologies. To take full advantage of its potential, careful optimization of the STI structure is required, making sure that the size of the isolation trench is adequate for the given doping profiles and isolation requirements.

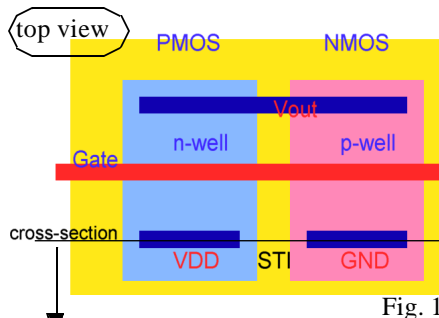


Fig. 1

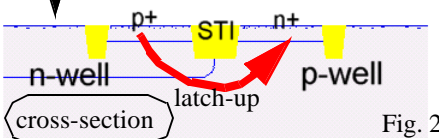


Fig. 2

A top view and a cross-section of a basic CMOS inverter are shown in Figs. 1, 2 respectively. Isolation properties of STI are characterized by calculating the triggering voltage of the parasitic p+npn+ thyristor structure. The latch-up path is indicated by the red arrow in Fig. 2.

### SIMULATION SETUP

A parametrized two-dimensional simulation structure, mesh and doping were set up for the simulation as shown in Fig. 3. Also shown is the electric potential in

the structure at zero bias (Fig. 4) and the doping profile (Fig. 5). High built-in

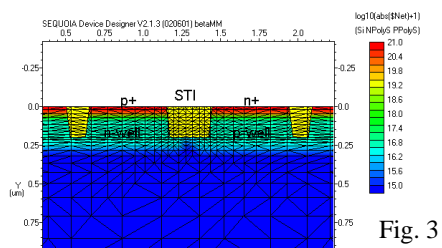


Fig. 3

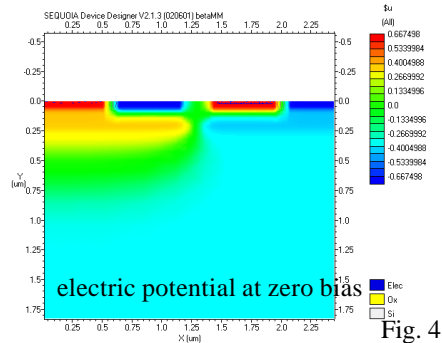


Fig. 4

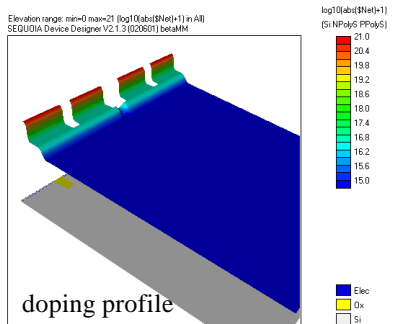


Fig. 5

potential in n-type regions (n-well and n+) is seen in red colors. Automatic meshing and parametrization of the structure allow in-depth studies of the STI properties with respect to geometry and doping parameters with little user effort (Figs. 6, 7).

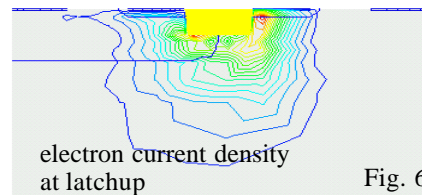


Fig. 6

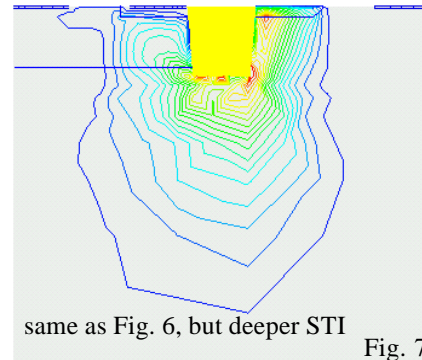


Fig. 7

### TRANSIENT LATCHUP

Transient simulations were carried out ramping up the potential applied to the VDD node. STI latch-up was considered to have occurred when a current level of 0.01A/micron was reached. At this current, a conductive path between p+ and n+ regions has fully developed. Such

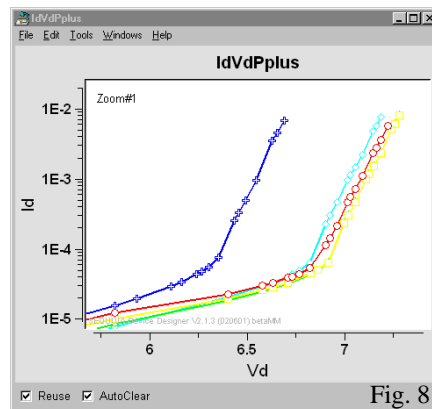


Fig. 8

simulations were repeated for different STI configurations to examine corresponding changes in trigger voltage.

### STI DEPTH AND WIDTH

As an example, a full-factorial experiment varied STI depth and width with three settings each: 0.3, 0.45, 0.6 $\mu\text{m}$ . A transient latch-up simulation was performed for each of the 9 settings (Fig. 8).

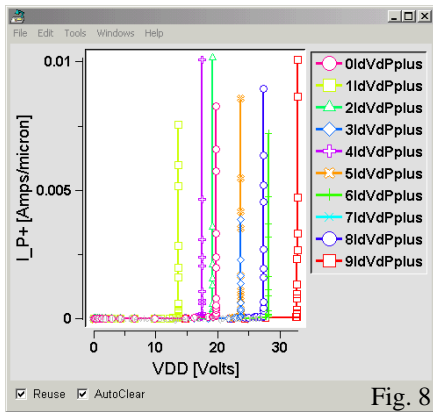


Fig. 8

Trigger voltages were extracted from each transient simulation and summarized in Fig. 9. As expected, results show that both increases in depth and in width improve latch-up susceptibility of STI. Sensitivity to other parameters, such as well depth and doping level, STI sidewall slope, etc., can be easily included in the analysis to arrive at an optimal STI configuration.

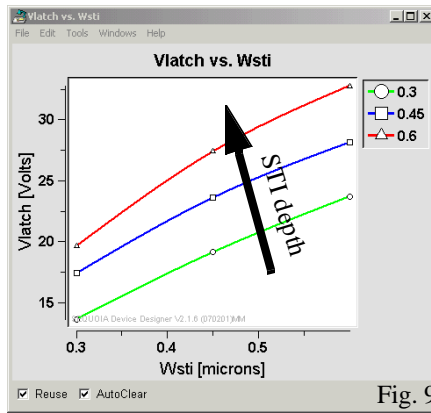


Fig. 9

### STI MANUFACTURABILITY

Another example of an STI study is the analysis of manufacturability with respect to mask layer misalignment. Since a certain degree of misalignment between the isolation mask layer and the n/p wells is unavoidable, excessive sensitivity of latch-up voltage to misalignment can lead to yield losses.

As shown by the latch-up voltage versus misalignment curve, the dependence is asymmetrical. The positive misalignment direction (n-well shifting to the right, see figure above) degrades isolation properties more severely than the negative misalignment direction (left).

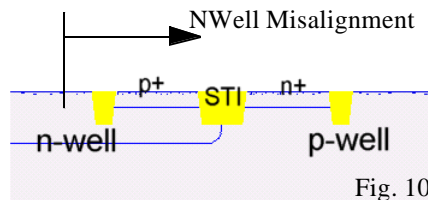


Fig. 10

### SUMMARY

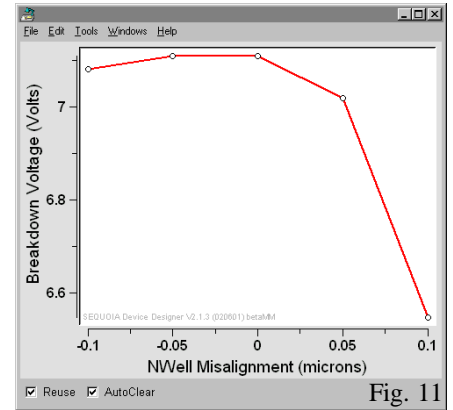


Fig. 11

Optimal design of Shallow Trench Isolation structures is important for high yields and efficient silicon area utilization. STI analysis and optimization involves performing a number of transient latchup simulation under varying design parameters such as geometry and doping.

SEQUOIA Device Designer offers a complete integrated software solution for the analysis and design of STI structures. Physical accuracy and ease-of-use are combined in a uniquely powerful package. For more information please contact SEQUOIA Design Systems.

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