

Device Synthesis with SEQUOIA Device Designer

Device synthesis is an increasingly popular approach to constructing TCAD models of semiconductor devices. The basic idea is to use a parametrized description of a device, where all structure and doping profile components can be easily adjusted. The parameters are, as far as possible, chosen to be directly observable quantities such as e.g. poly gate length, oxide thickness, spacer width, etc. for a MOSFET.

This approach allows us to depart from traditional TCAD-based device optimization methodology. This methodology is characterized by the use of coupled process-device simulation in an attempt to create a complete model of the semiconductor factory (so-called virtual factory). The motivation for this effort is the hope that actual fab experiments (split lots) can be replaced by “virtual” runs in simulation. Once this model has been established, an attempt is made to adjust the available process control settings to arrive at the desired device properties.

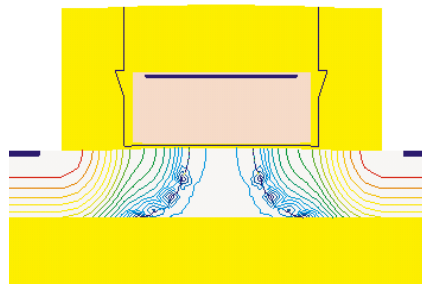
Unfortunately, constructing a model of required completeness and accuracy is a challenging task. The factory model is controlled by thousands of parameters including the process control settings, equipment attributes and, very importantly, process simulator parameters. The setting up of a “virtual factory” is a time-consuming and error prone task, which must include calibrating physical models encapsulated in the process simulator. These are several orders of magnitude more parameters than

the number of available measurements, making this “tuning” of parameters severely underdetermined. In addition, coupled process-device simulation is extremely time consuming and rather complex, making this approach unpopular among fab engineers.

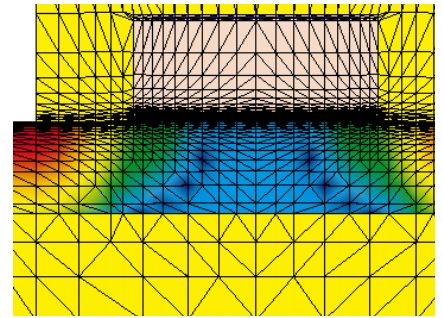
The synthesis approach, on the other hand, decouples finding the optimal device structure from establishing a process flow to achieve this structure. Using a parametrized device structure, a set of parameters is found which produces the desired electrical performances. Since the number of structure and doping parameters is similar to the number of available electrical measurements (typically less than 5-10), this optimization problem is well-balanced and solvable.

After the optimal device structure has been established, the process control settings are determined as a separate step, which must be supported by experiments.

The resulting device optimization strategy is a two-step process, which allows to fully explore all device architecture possibilities and find the optimal device structure in a very short time. Especially in



combination with inverse modeling techniques, the synthesis approach delivers quantitative accuracy and largely eliminates the need for simulator calibration.



The figures above show an SOI MOSFET device structure and mesh created from its parametrized description by SEQUOIA Device Designer.

	LDD	CH1	Ioff	Vth
Run0	4e18	6e17	6.5556e-013	0.64086
Run1	3.33e+018	4.461e+017	6.6557e-012	0.54346
Run2	2.056e+018	3.998e+017	4.7271e-012	0.52794
Run3	1.758e+018	3.95e+017	3.6823e-012	0.53177

With this parametrized device structure, built-in optimization can be used to determine the parameter values for desired electrical performance. As a simple example, the figure above shows how channel implant and LDD are simultaneously optimized to match targets set for Ioff and Vth.

SEQUOIA Device Designer is a complete, easy-to-use and fast integrated TCAD system based on device synthesis. It allows to quickly and accurately find the best device with the desired electrical performance.